SERVICE MANUAL

C286-LT

OCTOBER, 1990 **PN-400400-01**

Commodore

Produced By:

Commodore International Spare Parts GmbH
Braunschweig, West Germany

SERVICE MANUAL

C286-LT

OCTOBER, 1990 **PN-400400-01**

INTERNATIONAL EDITION

COMMODORE "INTERNATIONAL EDITION" SERVICE MANUALS CONTAIN PART NUMBER INFORMATION WHICH MAY VARY ACCORDING TO COUNTRY. SOME PARTS MAY NOT BE AVAILABLE IN ALL COUNTRIES.

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SECTION 1

SPECIFICATIONS

1.1 TECHNICAL SPECIFICATIONS

C286-LT	**AT Compatible**
MEMORY	
RAM on board	1MB: 640 KB Base memory, 384 KB extended/expanded memory; configurable by user
VIDEO RAM	256 KB (A000:0000H-13000;FFFH): 32 KB (frame buffer for LCD)
ROM	128 KB (64 KB for system BIOS, 64 KB for VGA video BIOS)
RAM EXPANDABLE	
on board	Yes; to 5M — 2 meg. memory expansion cards optional (maximum of two cards for a total of 5 meg.)
CPU	
Type	80C286
Clock speed	12.5 MHz, 8 MHz
EXTERNAL STORAGE	
Floppy disk drive	
Type	3.5-inch double-sided high density
Supported disks	3.5-inch 1.4 MB, 3.5-inch 720 KB
Hard disk	
Capacity	20 MB
Type	2.5-inch, low power consumption type
Access time	23 ms mean access time
Interface	IDE
DISPLAY	
Dimensions	197 mm x 149 mm (7¾" x 5⅞") diagonal 247 mm (9¾") 0.27 mm dots size and 0.3 mm dot pitch 1:1 aspect ratio
Type	STN type LCD with CFL backlight lamp
Video mode	Compatible with VGA Text: 80 characters x 25 lines or 40 characters x 25 lines Graphics: 640 x 480
Gray scale	8 shades of gray
AC ADAPTER	
Input	Operating voltage — 100 to 240 VAC Frequency — 50/60 Hz
Output power	Adapter mode — 24 W Charger mode — 45 W
Input current	Adapter mode — 0.6 A Charger mode — 1 A
Dimensions	85 W x 205 D x 55 H mm
Weight	0.65 Kg
SOFTWARE	
Operating System	MS-DOS 4.01 with Shell
Language	GW-BASIC
Utilities	
Eagle.com	LCD control
Switcher.com	LCD control
Alarm.com	Indicating low battery
Mdmon.com/mdmoff.com	Modem power on/off

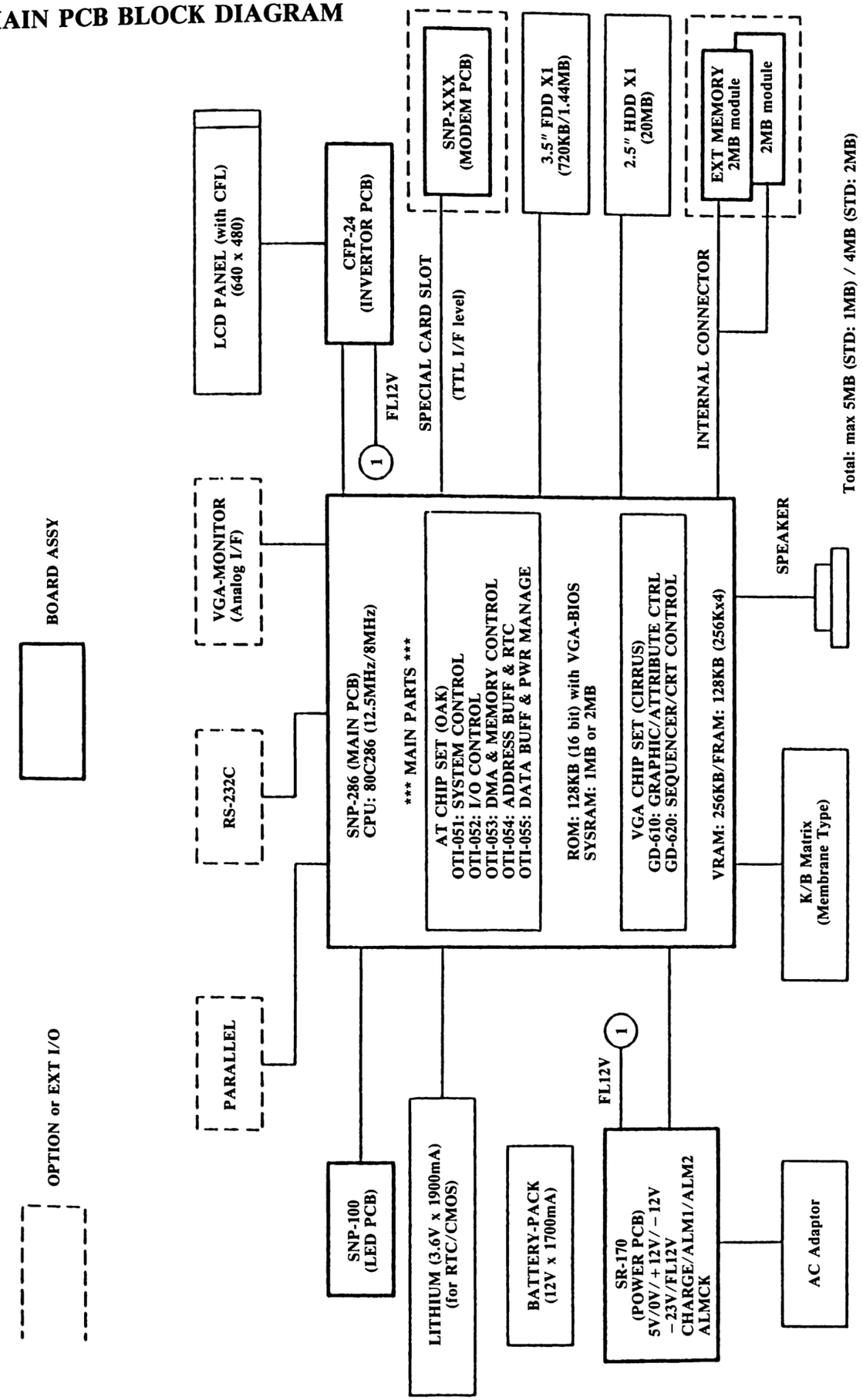
SECTION 2

THEORY OF OPERATIONS

NOTE

PLEASE REFER TO C286-LT OPERATIONS MANUAL PN-363573-01 FOR ADDITIONAL INFORMATION

2.1 MAIN PCB BLOCK DIAGRAM



2.1 — MAIN PCB BLOCK DIAGRAM

2.2 MAIN SYSTEM PARTS

SYSTEM CONTROL OTI-051

I/O CONTROL OTI-052

DMA & MEMORY CONTROL OTI-053

ADDRESS BUFFER & RTC OTI-054

DATA BUFFER & POWER MANAGER OTI-055

SYSTEM CLOCK OTI-051

DMA CHANNEL ASSIGNMENT

Channel 0 - Not used
Channel 1 - Not used
Channel 2 - Floppy Disk Controller
Channel 3 - 4 Not used
Channel 5 - 7 Not used

INTERRUPT CONTROL OTI-052

INTERRUPT CONTROLLER CHANNEL ASSIGNMENT

IRQ 0 - Timer Channel 0
IRQ 1 - Keyboard Interface Interrupt
IRQ 2 - Not used
IRQ 3 - Com2 Interrupt
IRQ 4 - Com1 Interrupt
IRQ 5 - Not used
IRQ 6 - Floppy Disk Controller Interrupt
IRQ 7 - Printer Interface Interrupt
IRQ 8 - Real Time Clock
IRQ 9 - Not used
IRQ10 - Power Saving Mode
IRQ11 - 13 Not used
IRQ14 - Hard Disk Controller Interrupt
IRQ15 - Not used

BUS CONTROLLER OTI - 051

TIMER/COUNTER OTI - 052

TIMER/COUNTER CHANNEL ASSIGNMENT

Channel 0 - System Timer for use with MS-DOS
Channel 1 - Memory Refresh Timing Generator
Channel 2 - Speaker Beep Tone Generator

KEYBOARD/SENSE CONTROL PORT 80C42

OUTLINE OF OTI-051

The OTI-051 is a customized IC in the Oak Model 35 chip set and it is a system control chip used in IBM AT and Model 30-286 architectures. Its main features are described below.

System Control	8 MHz, 10 MHz, 12.5 MHz, 16 MHz and 20 MHz system speeds supported
I/O Channels	8 MHz asynchronous mode, and 8 MHz, 10 MHz and 12 MHz synchronous modes Programmable wait state
Laptop	Power management function
Other Features	Fast reset and time-out counter

2.2 MAIN SYSTEM PARTS (Continued)

OUTLINE OF OTI-052

The OTI-052 is an I/O peripheral controller circuit which comes with the following functions.

- Two 8259-compatible interrupt controllers
- 8254-compatible timer/counter
- 16450-compatible serial communication controller
- Floppy disk controller, hard disk subsystem, keyboard controller, numerical calculation processor and other chip select circuits
- Numerical calculation processor interface circuit

OUTLINE OF OTI-053 DMA & MEMORY CONTROLLERS

The OTI-053 is an integrated circuit which has a DMA controller and memory controller, and its main features are listed below.

- 0 wait cycle page mode and interleave mode
- DRAMs with access times ranging from 60ns to 120ns supported
- System speeds up to a maximum 20 MHz
- Programmable wait state for slow-speed DRAMs
- Non-wait state ROM cycle execution enabled with use of shadow RAM
- EMS4.0 supported
- 640KB system memory and total memory space of up to 8MB using extension/expansion memories supported
- 256KB and 1MB type DRAMs supported
- Dummy SRAM for laptop models supported
- Cartridge ROMs supported

DMA Control

- Fast and normal DMA modes with built-in 8237 to handle operating speeds up to 10 MHz

Laptop Support

- Power-saving mode

OUTLINE OF OTI-054

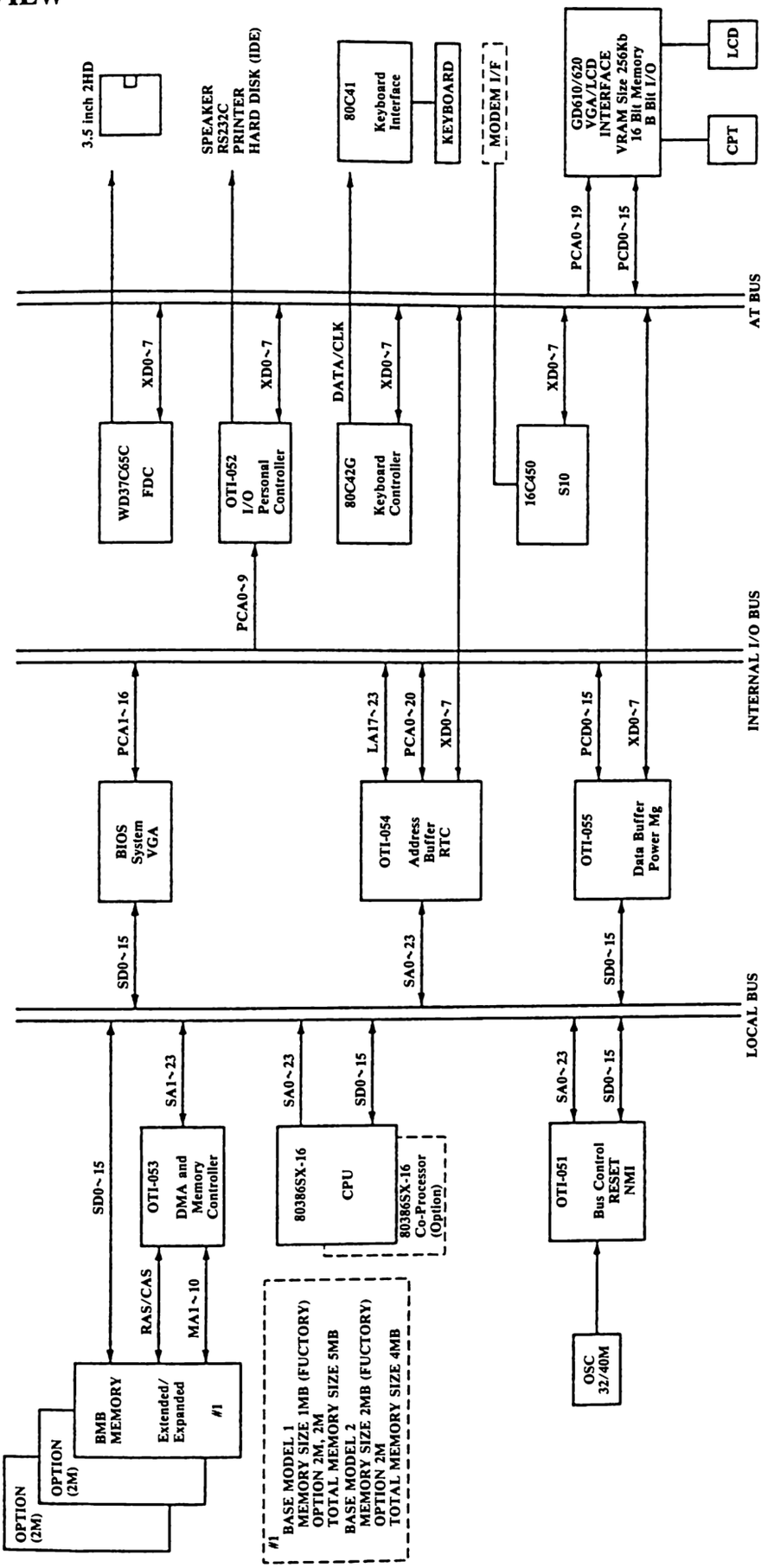
The OTI-054 is a customized IC in the Oak Model 35 chip set and it is an address buffer driver for IBM AT, Model 30 and other 286-compatible systems. It features all the TTL address and command driver functions normally required on a system board. In addition to its address driver functions, it comes with an RTC (real-time clock) function. Except for the 3 items below, the RTC function is compatible with the MC146818.

- 128-byte CMOS RAM in total
- No CKFS (clock-out frequency select) input facility
- No SQW (square wave) output facility

OUTLINE OF OTI-055

The OTI-055 features all the TTL data driver functions normally required on a system board and, in addition to its data buffer functions, it comes with power manager functions for laptop computers. It has 16 bidirectional control/status signal lines which can be used by system designers to control power distribution to peripheral units inside a system. Besides these 16 signal lines, it features an internal timer/counter which enables the user to supply power automatically to the system.

2.3 SYSTEM OVERVIEW

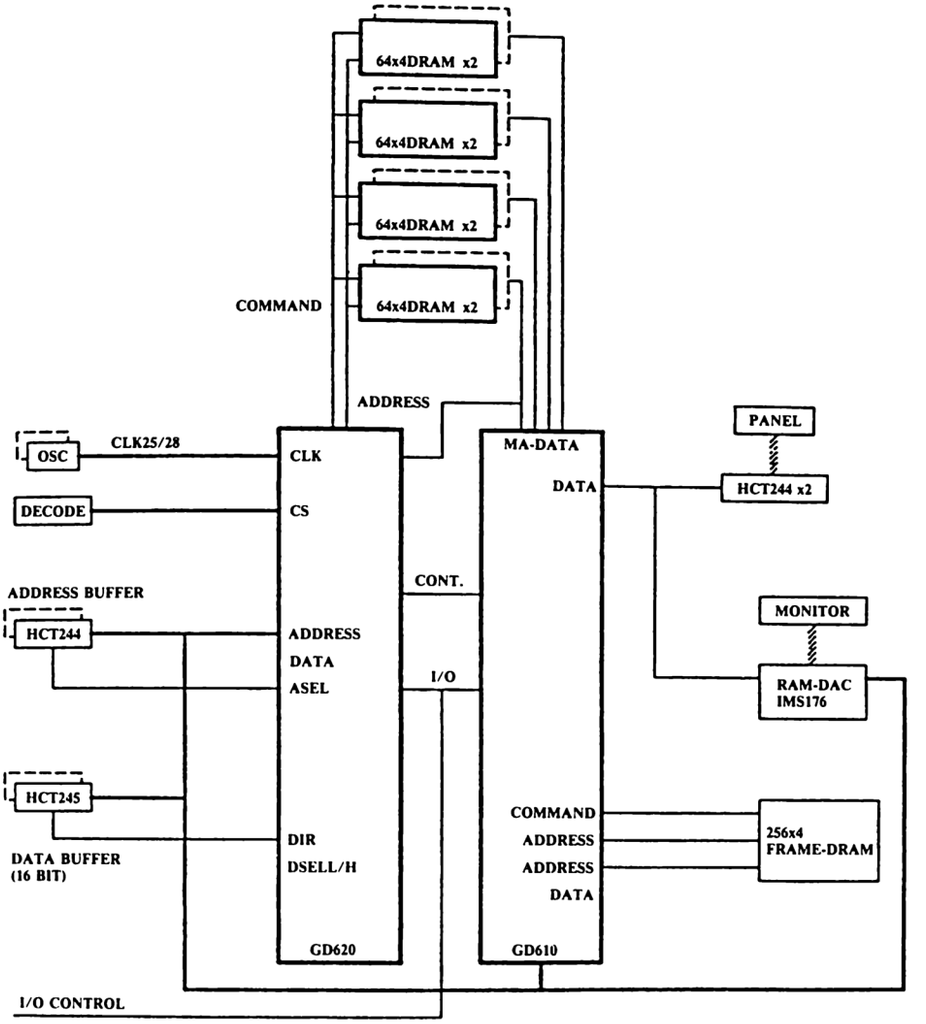


2.2 — SYSTEM OVERVIEW

2.4 DISPLAY

CONTROL DEVICE	Graphics/Attributes CL-GD610; Sequencer CL-GD620
GRAPHIC RESOLUTION	620 x 480 Dots
CHARACTER DISPLAY	80 Character x 25 Line or 40 Character x 25 Line
EMULATION MODE	CGA, EGA, MDA, and Hercules (register level)
DISPLAY DEVICE	The following devices can be used: LCD Panel; (8 GRAY SCALES); CRT with external Analog output; (64 GRAY SCALES at MDA mode); (16 colors 640 x 480); (256 colors 320 x 200) At the boot-up, LCD Panel is always enable. You can change LCD Panel, or External CRT by Utility software (Eagle. com/Switcher .com) *NOTE:* VGA BIOS loads the appropriate parameter, after recognizing which monitor is connected, Color or Monochrome. When power switch is turned to on and no monitor is connected, VGA BIOS sets its parameter for monochrone monitor.
DISPLAY CONTROL	VGA mode
VIDEO RAM	256K Bytes + frame buffer 32K Bytes
VIDEO RAM ACCESS	The Video RAM can be accessed completely in the same way as accessing normal memory RAM, from CPU. Write and Read functions are freely executed without checking the status of the display control device.
CHARACTER GENERATOR	Character ROM is stored in the Video Bios and used for the character display mode (US ASCII ver.).
BASE SYSTEM DISPLAY DEVICE	Consists of STN LCD (blue) panel with CFL back light. In addition, the display can be switched to the analog CRT (color/ monochrome) output by software.
AFFECTIVE DISPLAY AREA	
Display Size	197mm x 149mm
Dot Size	0.27mm x 0.17mm
Dot Pitch	0.3mm x 0.3mm
Aspect Ratio	1:1
CFL/LCD Auto OFF	If you close the panel while power switch is on, the CFL and LCD Panel will be automatically shut off.
BACKLIGHT BRIGHTENERS	Backlight brightness can be set high (3.2W), or LOW (1.5W) by SETUP MENU.
CFL BACKLIGHT LIFE	About 8,000 hours (condition: within the max. rating)

2.5 VGA SYSTEM BLOCK DIAGRAM



2.3 — VGA SYSTEM BLOCK DIAGRAM

CONNECTOR: 15 Pin D-sub (male)

CONNECTOR PIN ASSIGNMENT

PIN NUMBER	*DESCRIPTION*	*PIN NUMBER*	*DESCRIPTION*
1	Red	9	Reserved
2	Green	10	Ground
3	Blue	11	MS0*
4	MS2*	12	MS1*
5	Ground	13	Horizontal sync.
6	R Ground	14	Vertical sync.
7	G Ground	15	Not connected
8	B Ground		

*MS0-MS2 are used for sensing a type of monitor.

2.6 FLOPPY DISK DRIVE AND CONTROLLER

FLOPPY DISK DRIVE	
Type	FD-334HF; 3.5 inch double side drive
Data Capacity	1.44M/720K Bytes (formatted) 2M/1M Bytes (unformatted)
Data Transfer Rate	500K bits/sec/250K bits/sec
Track Density	135 tpi
Required Power	+5V Single (4.6 - 5.5V)
Track to Track Time	3msec
Disk Rotation Speed	300rpm
LED Indicator	Green
Width	101.6mm
Height	19mm
Depth	135mm

Current and Power Consumption

	Typ. current	*Typ. power*
Standby	10.0mA	50mW
Read Operation	0.40A	2.0W
Write Operation	0.42A	2.1W
Motor Start	0.07A	3.5W

FLOPPY DISK CONTROLLER	WD37C65B
Data Transmission	DMA transmit
Transfer Rate	High Density — 500K bit/sec. Normal Density — 250K bit/sec.

2.7 HARD DISK DRIVE

Type	CP2024; 2.5 inch 20M Bytes Hard Disk
Data Capacity	21.4M Bytes (formatted)
Data Transfer Rate (Media)	1.25 MB/sec
Data Transfer Rate (Buffer)	3.75 MB/sec
Seek Time	Track to Track — 5ms Average — 23 ms Maximum — 40ms
Rotation Speed	3,433rpm
Total Tracks	1,306
Cylinders	653
Disks	1
Data Heads	2
Width	69.8mm
Height	17.5mm
Length	101.6mm
Power Requirement	+5V ±5% 600mA (Typ.r/w)

2.8 PARALLEL PRINTER INTERFACE

CONTROL Printer handshaking is controlled by STROBE, and BUSY signals.

OUTPUT Standard TTL input printers can be used, such having TTL input. When the printer is used, the connector can be plugged in or removed without destroying the inner circuits of the devices regardless of power ON/OFF.

PARALLEL CONNECTOR D shell 25P (female)

PARALLEL CONNECTOR PIN ASSIGNMENT

PIN NUMBER	*DESCRIPTION*	*CONTENTS*	
1	OUTPUT	STROBE	STROBE Signal
2	OUTPUT	PDB 0	Print data bit 0
3	OUTPUT	PDB 1	Print data bit 1
4	OUTPUT	PDB 2	Print data bit 2
5	OUTPUT	PDB 3	Print data bit 3
6	OUTPUT	PDB 4	Print data bit 4
7	OUTPUT	PDB 5	Print data bit 5
8	OUTPUT	PDB 6	Print data bit 6
9	OUTPUT	PDB 7	Print data bit 7
10	INPUT	ACK	Printer acknowledge
11	INPUT	BUSY	Printer busy
12	INPUT	P.end	Out of paper
13	INPUT	SELECT	Printer select
14	OUTPUT	ATF	Auto feed
15	INPUT	ERROR	Printer error
16	OUTPUT	INIPRN	Initialize Printer
17	OUTPUT	SELINP	Select input
18 - 25		GND	

2.9 RS-232C INTERFACE

STANDARD EIA standard

DEVICE OTI-052

OUTPUT SIGNAL LEVEL Output signals based on ±12V supplied voltage.

INPUT SIGNAL VOLTAGE SPACE = +3V, +15V
MARK = −3V, +15V

BAUD RATE (50), (75), 110, 150, 300, 600, 1200, 2400, 4800, 9600

NOTE: The values in ( ) are not supported by software (INT 14h). They need to be directly accessed by software.

CONNECTOR 9 Pin D-sub (male)

SERIAL CONNECTOR PIN ASSIGNMENT

PIN NUMBER	*SIGNAL*	*DESCRIPTION*
1	CD	Carrier Detect
2	RxD	Receive Data
3	TxD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Signal Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	RI	Ring Indicator

2.10 MODEM I/F SLOT

CONNECTOR 20-Pin Connector Edge Socket

STANDARD AND SIGNAL LEVEL Based on RS-232C, TTL Level

MODEM CONNECTOR PIN ASSIGNMENT

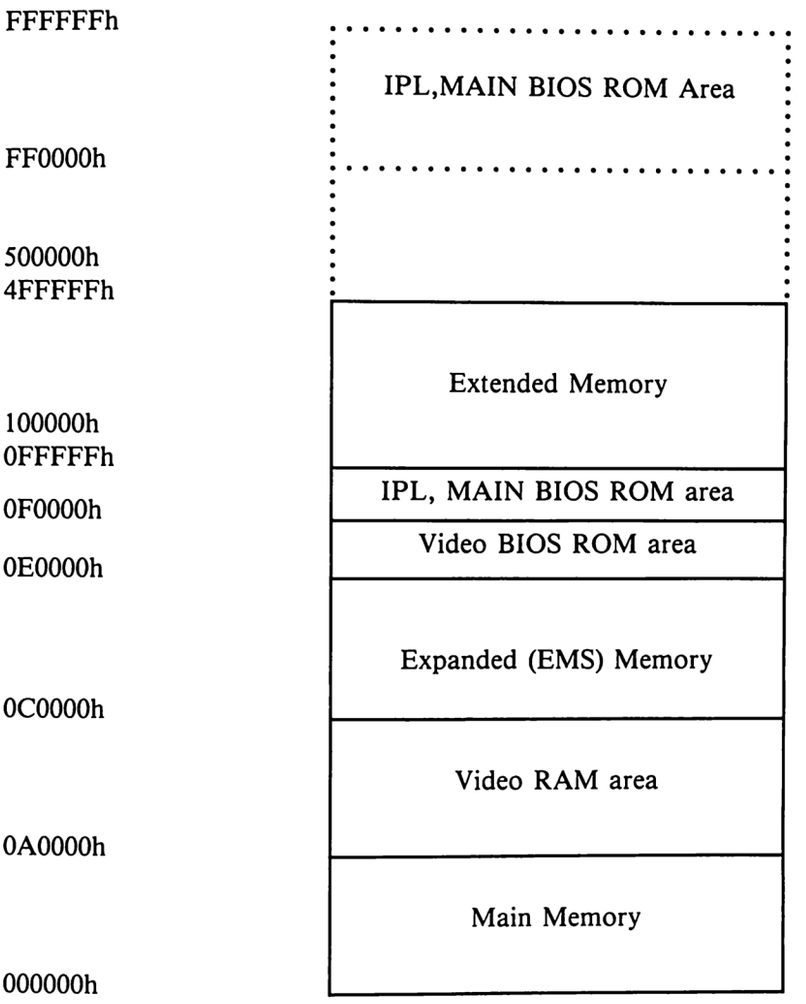
PIN NUMBER	*SIGNAL NAME*
A1	CONTROLLED 5 Volt
A2	CONTROLLED 5 Volt
A3	RTS
A4	DTR
A5	TXD
A6	DSR
A7	RI
A8	DCD
A9	CTS
A10	RXD
B1	– 12V
B2	GND
B3	GND
B4	GND
B5	GND
B6	GND
B7	GND
B8	GND
B9	GND
B10	GND

2.11 C286-LT MEMORY MAP

The C286-LT has available 1 MB of RAM. Base memory is 640 KB (kilobytes) and 384 KB is allocated for extended memory. By adding Commodore 2 MB RAM modules, memory may be augmented to a total of 5 MB.

By using MS-DOS 4.01 features, a portion or all extended memory can be used to emulate expanded memory conforming to the LIM 4.0 specification.

Extended memory can be utilized by many applications and operating systems functioning in protected and standard modes.



2.4 — MEMORY MAP

2.12 I/O ADDRESS MAP

I/O ADDRESS	*R/W STATUS*	
0000h-000Fh	R/W	DMA controller 1, 8237A
0010h-0018h	R/W	EMS register
001Eh-001Fh	R/W	OAK special register
0020h-003Fh	R/W	Interrupt controller 1, 8259A, Master
0040h-005Fh	R/W	Timer, 8254
0060h-006Fh	R/W	80C42 (Keyboard), System control register
0070h-007Fh	R/W	Real-time clock, NM1 (non-maskable interrupt) mask
0080h-008Fh	R/W	DMA page register
0094h	R/W	System board setup enable register
00A0h-00BFh	R/W	Interrupt controller 2, 8237A
00C0h-00DFh	R/W	DMA controller 2, 8237A
0102h	R/W	POS register 2
01F0h-01F7h	R/W	Fixed Disk 0
0278h-027Fh	R/W	Parallel port 3
02F8h-02FFh	R/W	Serial port 2
0378h-037Fh	R/W	Parallel port 2
03B0h-03BFh	R/W	Video Graphics Adapter 1 and Parallel port 1
03C0h-03CFh	R/W	Video Graphics Adapter 1
03D0h-03DFh	R/W	Video Graphics Adapter 1
03F0h-03F7h	R/W	Floppy Disk A
03F8h-03FFh	R/W	Serial port 1

SECTION 3

TROUBLESHOOTING

3.0 TROUBLESHOOTING SECTION

1) DISASSEMBLY INSTRUCTIONS FOR FIELD REPLACEMENT UNITS

2) POWER ON DIAGNOSTIC TESTS

CAUTION

USE ANTI-STATIC PRECAUTIONS
WHEN SERVICING THIS PRODUCT

DISASSEMBLY INSTRUCTIONS FOR C286-LT

3.1 KEYBOARD REMOVAL INSTRUCTIONS

Remove the three screws (1) from Bottom Cabinet (the cabinet bottom). (Figure 3.1)
Fold up the LCD display.
Lift up Top Cabinet together with the keyboard in the direction indicated by the arrow.
NOTE: As the FPC cable is plugged into the connector, it must be lifted a little as well.
Unplug the FPC cable from the connector.
Remove the keyboard.

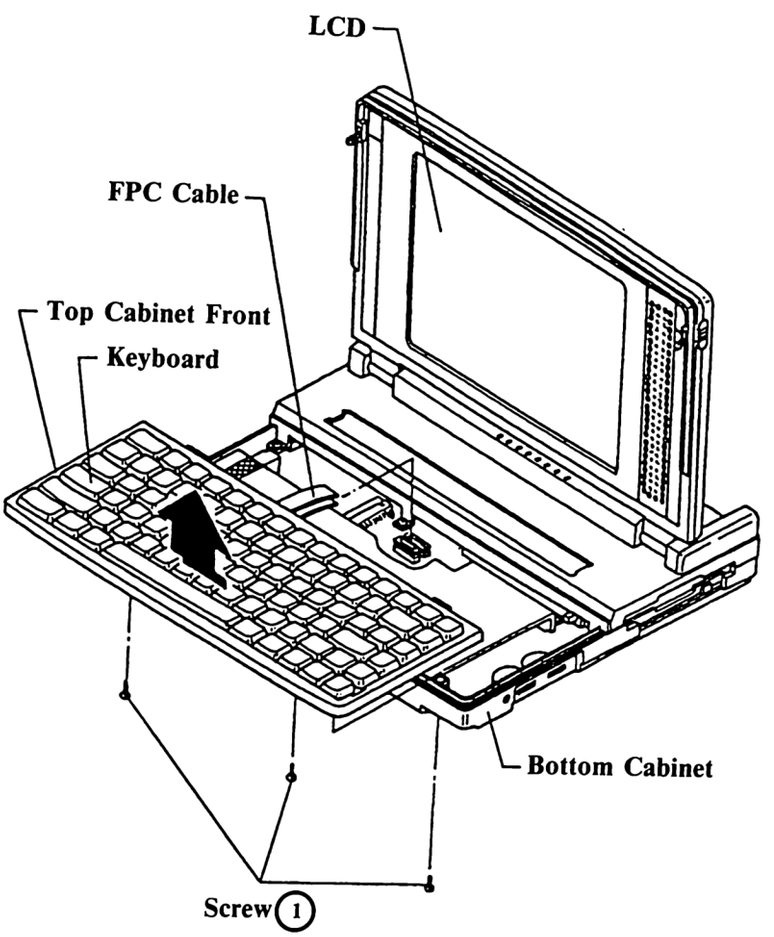


Figure 3.1

DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)

3.2 NICAD BATTERY PACK AND LITHIUM CELL REMOVAL INSTRUCTIONS

Push up on the Nicad battery pack lever in the direction indicated by the arrow. (Figure 3.2)
Remove the Nicad battery pack.
Slide Cover Backup Battery in the direction indicated by the arrow and remove it.
Take out the lithium cell and unplug the connector from it.
Remove the lithium cell.

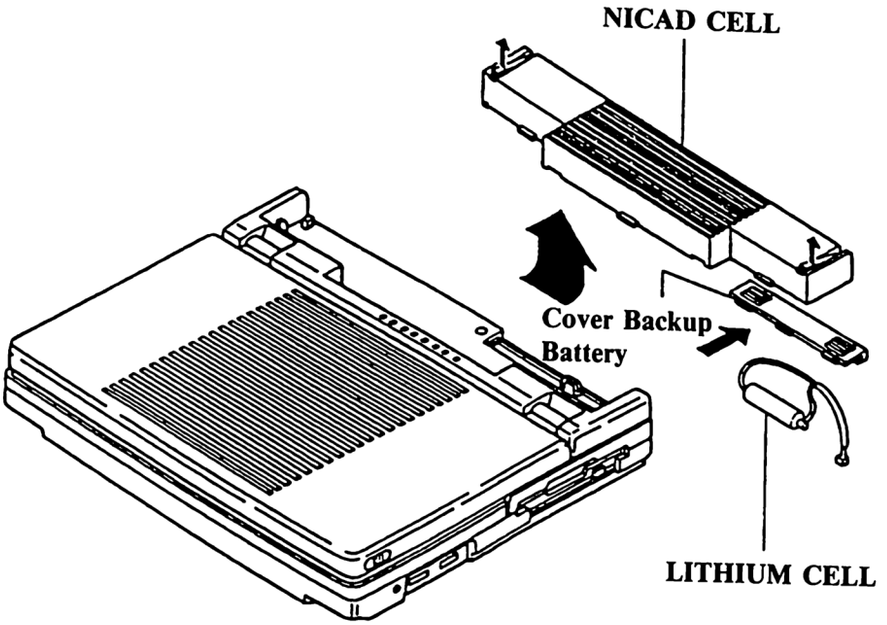


Figure 3.2

DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)

3.3 HDD REMOVAL INSTRUCTIONS

Follow the instructions under 3.1 to remove the keyboard.

Remove the three screws (1) which hold Shield HDD in place. (Figure 3.3)

Remove Shield HDD. Do not return Shield with defect drive.

Remove the four screws (2) from Bottom Cabinet (the cabinet bottom).

Unplug the HDD cable from the connector.

Remove the HDD.

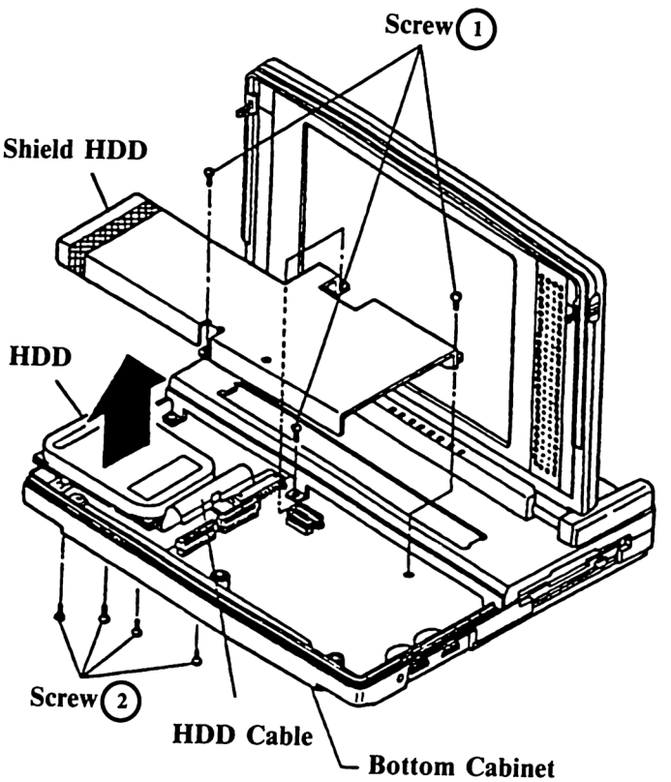


Figure 3.3

DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)

3.4 LCD POWER UNIT INVERTER REMOVAL INSTRUCTIONS

Follow the instructions under 3.1 to remove the keyboard.

Follow step 3.2 to remove the Nicad battery pack.

Remove the six screws (1) and (2) which hold Top Cabinet Rear in place. (Figure 3.4)

Unplug connectors (1) through (9) from the main PCB. See Wiring Diagram (Figure 3.8)

Remove LCD Unit.

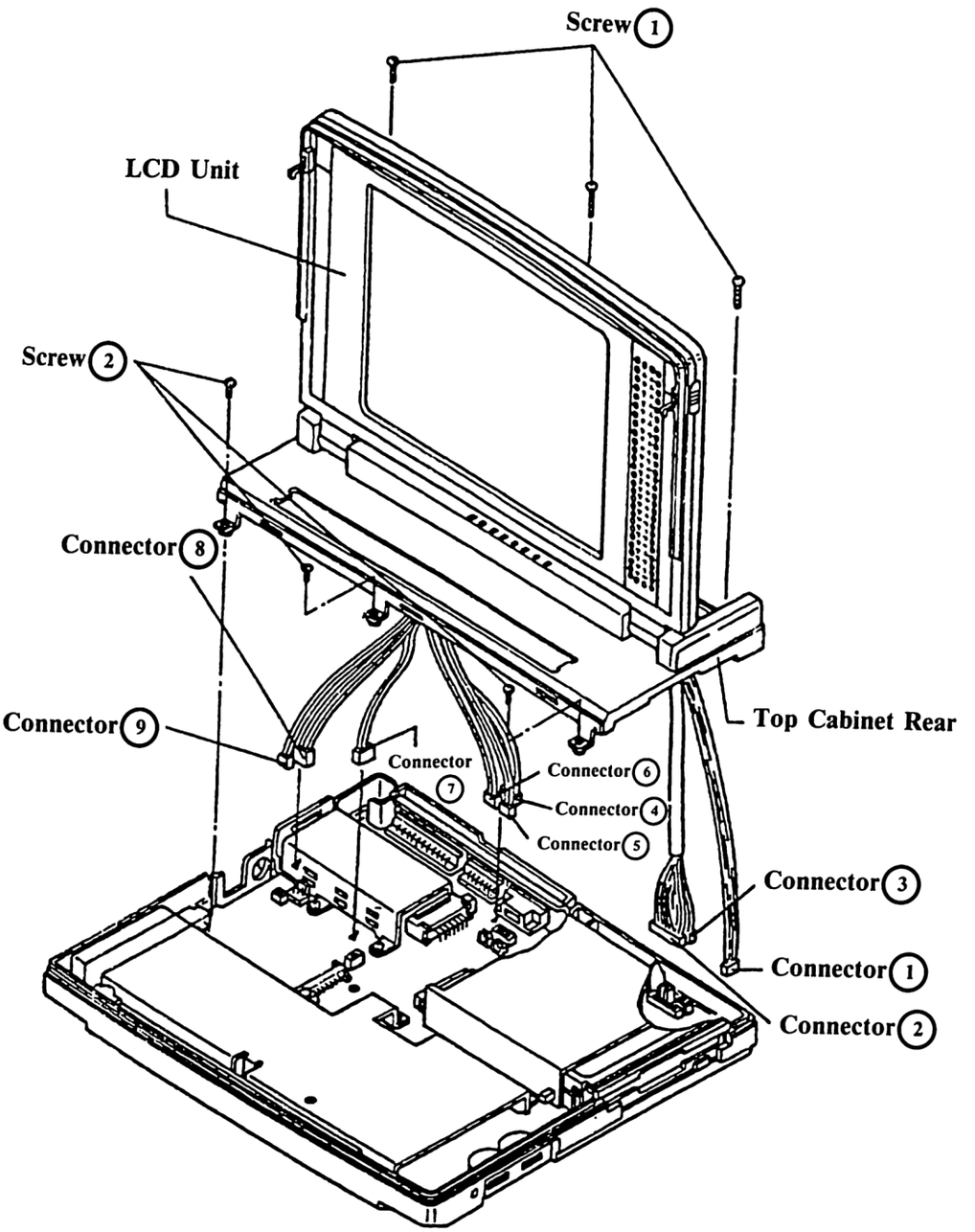


Figure 3.4

DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)

3.5 MAIN PCB, POWER SUPPLY PCB, FDD AND SPEAKER REMOVAL INSTRUCTIONS

Follow the instructions under 3.1 to remove the keyboard.

Follow step 3.2 to remove the Nicad battery pack.

Follow step 3.3 to remove Shield HDD and HDD.

Follow step 3.4 to remove LCD unit.

Remove the three screws (1) which hold Case Modem in place. (Figure 3.5)

Remove the two screws (2) which hold the main PCB in place.

Remove the main PCB and power supply PCB from Bottom Cabinet.

NOTE: When removing the main PCB from Bottom Cabinet, there is a knob that needs to be moved a little to the left to make room.

Pull the main PCB and power supply PCB apart.

Remove the four screws (4) which hold the main PCB and FDD in place.

Unplug connector (1) from the main PCB and FDD.

Remove the FDD.

Remove the speaker.

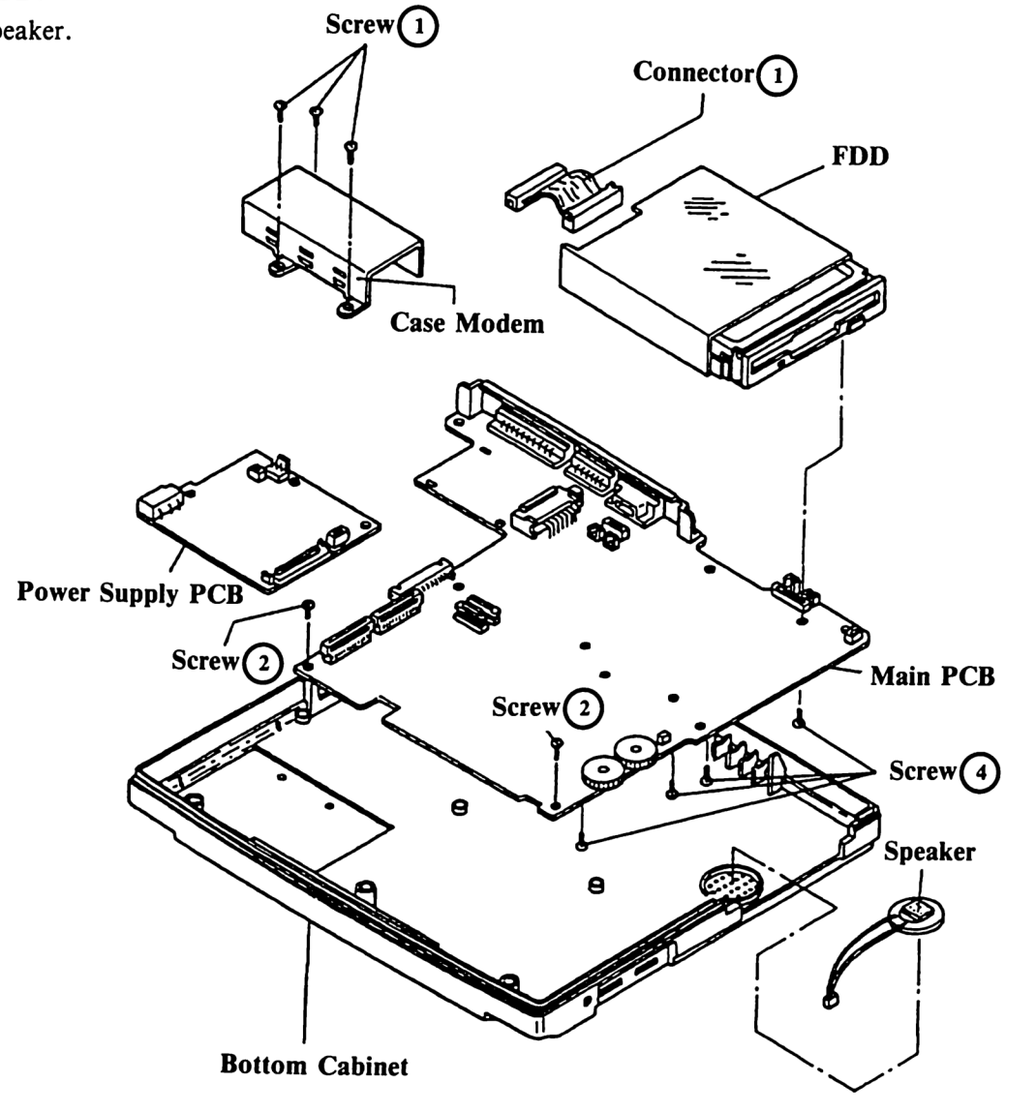


Figure 3.5

DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)

3.6 MEMORY PCB (OPTION) INSTALLATION

Follow the instructions under 3.1 to remove the keyboard.

Install the memory PCB in locations CN23, CN25 and CN26 on the main PCB (2 MB version). (Figure 3.6)

Install the memory PCB in locations CN23, CN25 and CN26 and CN24, CN27 and CN28 on the main PCB (4MB version). (Figure 3.7)

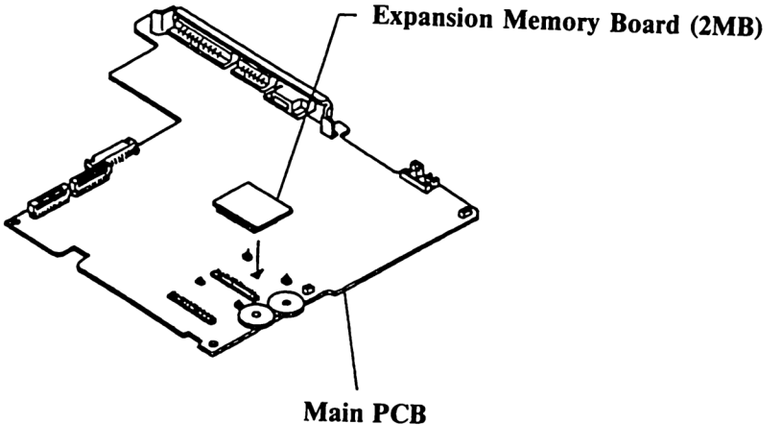


Figure 3.6

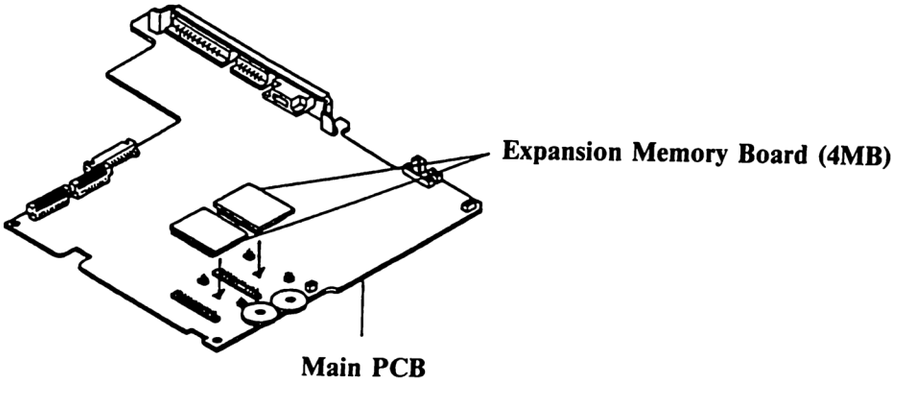


Figure 3.7

3.8 TROUBLESHOOTING ERROR MESSAGES

TROUBLESHOOTING GUIDE

Error Messages	Customer Response	Service POD Test (H)
1. DMA 1 error	See your dealer	Test 0B
2. DMA 2 error	See your dealer	Test 0C
3. Interrupt controller 1 error	See your dealer	Test 0D
4. Interrupt controller 2 error	See your dealer	Test 0E
5. PIO error	See your dealer	Test 0F
6. Parity error	See your dealer	Test 10
7. Real time clock is not working	See your dealer	Test 1E
8. Illegal shutdown code in CMOS	See your dealer	Test 02
9. Virtual Mode CPU error	See your dealer	Test 26
10. Parity error on main circuit board	See your dealer	Misc
11. Parity error on expansion bus	See your dealer	Misc
12. Non-recoverable error-Processor halted	See your dealer	Misc
13. Press F1 key to continue	Press F1 key	Misc
14. Battery Failure	Run Setup Utility/See your dealer	Test 11
15. Base memory configuration error	Run Setup Utility	Test 17
16. Extended memory configuration error	Run Setup Utility	Test 18
17. Floppy 0 configuration error	Run Setup Utility	Test 1A
18. Floppy 1 configuration error	Run Setup Utility	Test 1A
19. Coprocessor (80287) configuration error	Run Setup Utility	Test 1D
20. The realtime clock has not been initialized	Run Setup Utility	Test 1E
21. Keyboard	Check keyboard	Test 14
22. Key switch is off. Turn it on to continue	Turn keylock on	
23. Boot failure, check disk and hit any key to try again	Check for non-MS-DOS disk in Drive A:; run Setup Utility	Misc

PLEASE NOTE

THE FOLLOWING OVERVIEW OF POWER ON DIAGNOSTICS TESTS IS FOR INFORMATION ONLY. COMPONENT LEVEL REPAIRS TO THE C286-LT PCB ARE NOT AUTHORIZED BY COMMODORE.
SEE PCB REPLACEMENT PROCEDURES IN THIS SECTION.

3.9 POWER ON DIAGNOSTICS

C286-LT Troubleshooting

The Commodore 80286 ROM bios contains a "Power on Diagnostic" program which tests the functions of hardware and checks the configuration prior to passing control to the operating system.

The number of the test routine being run is passed to addr 03 78 (H) prior to the start of each test section.

The 80286 processor is initialized by the "RESET" signal. Refer to RESET description in IC pinout section, note that "VCC" and "CLK" to CPU must be correct and "HOLD" must not be active for 34 ticks from leading edge to trailing edge of initial reset.

RESET will terminate all instruction execution and local bus activity until it is negated. Prior to fetching, decoding and executing, the first instruction, located at physical address FF FF F0 (H), the 80286, in real address mode, processes some micro code located in its internal ROM, this takes about 38 ticks.

Test 01 (H) 0000 0001 (B)

The first test performed by the power on diagnostic checks the 8088 flags, the arithmetic logical unit, and the CPU registers.

If a failure is detected in Test 01, a "HALT" instruction is executed. This will stop program execution and prevent the CPU from using the local bus. The 80286 can be forced out of the halted state by "RESET", "NMI" or "INTR" (when "INTR" is used for RESTART, the interrupt enable bit of flag register must be on (set to 1), and the effective address computed from CS:IP will point to the next instruction after the halt instruction).

***Failure in test 01 indicates defective 80286.

Test 02 (H) 0000 0010 (B)

This routine checks to see if a "SHUTDOWN" has occurred. A shutdown can indicate a severe error which would prevent the CPU from further processing.

NOTE: A halt or shutdown condition is signaled externally, by the 80286 as a bus operation. Low states on S0', S1', COD/INTA', and a high state on M/IO' indicate a halt or shutdown. The state of address line 1 will indicate which condition, A1 high is halt, A1 low is shutdown.

After the test number is moved to the parallel port a check for keyboard reset is conducted and the program branches to test 04 (H) if it has.

The check for shutdown begins by examining the 8242 keyboard controller status port. In all ten shutdown conditions are tested, of these, three unexpected shutdown conditions, numbers 6, 7 or 8, any one of which if true, will generate the console message:

"Illegal Shutdown Code in CMOS"

NOTE: Branch information for shutdown routines are stored in CMOS memory. The shutdown command is sent to the 8242, the UPI status port, which will halt the CPU. Return depends on the shutdown code in CMOS memory.

An error code, F6, F7 or F8, (HEX) is sent to the parallel port before calling the display routine which generates the above message.

In real address mode a shutdown could occur under the following conditions:

Interrupt number 8, interrupt number 13, or a "CALL INT" or "PUSH" instruction which wraps stack segment when SP is ODD.

Routines also perform valid shutdowns to exit protected mode. During these the DMA page register will be initialized and interrupt control words (ICW) 1, 2, 3 and 4 will be reinitialized. Other routines within the test enable "NMI", parity and set the I/O check bit.

***Failures in test 02 could indicate problems on the local bus, or expansion bus. This would include: 80286, OTI-051, OTI-053, OTI-052, or any third party cards.

Test 03 (H) 0000 0011 (B)

Eprom checksum test verifies contents of eprom by adding bytes and checking for result of zero. A compensation byte is factored into the addition to make the sum zero.

Detection of an error results in a halt condition and would invalidate tests 01 and 02.

***Failure in test 03 indicates defective ROM.

Test 04 (H) 0000 0100 (B)

Test 04 checks the DMA page registers by writing and reading bits starting at address 80 (H).

***Failure in test 04 indicates possible defective OTI-053, OTI-052, or local bus.

Test 05 (H) 0000 0101 (B)

Timer 1 and timer 2 are checked for correct operation. Interrupts are masked off during the test.

***Failure in test 5 indicates possible defective OTI-053, OTI-052.

Test 06 (H) 0000 0110 (B)

Memory refresh test. Timer and DMA are setup to initiate refresh cycles every 15.1 microseconds. Size of virual memory is calculated.

***Failure in test 06 indicates possible OTI-053, OTI-052, Refresh logic or memory problem.

Test 07 (H) 0000 0111 (B)

Test 07 checks the 8242 keyboard controller by writing and reading the keyboard buffers.

***Failure in test 07 indicates possible defective 8242 or associated circuitry.

Test 08 (H) 0000 1000 (B)

Test 08 writes and reads the first 128K of RAM and verifies block size is 128K. First pass writes addresses into data, the second pass writes the complement of the address into data. Memory is cleared after test. The battery status is also confirmed in test 08.

***Failure in test 08 indicates possible defective RAM or RAM logic.

Test 09 (H) 0000 1001 (B)

Test and configure video. A search is made to determine if MDA, CGA or a special video adapter is configured, if not the onboard VGA is enabled and a call to VGA bios is executed. The dip switches are read to determine the default video mode.

NOTE: The mode register setting in the GD610 controls the reset signal to the onboard VGA controller chip. If no special video adapters are found on the expansion bus then "NOVID" from the GD610 is negated.

On completion of this test the title and copyright message are displayed.

Test 0A (H) 0000 1010 (B)

Test RAM from 128K to 640K. A display message is generated indicating that the base RAM of 128K, Test 08, is OK.

Blocks of 128K, starting at 128K are then tested by writing, reading and verifying RAM. The first pass writes addresses to data, that is, the address which defines the physical location is also used as the bit pattern that is being written. The second pass writes complement of address into data.

The test displays results in blocks of 128K to the console each time a 128K boundary is reached.

At completion of the onboard memory test the CPU is placed in virual mode and a test for virtual memory (over 1 MEG) is started.

NOTE: See test 26 (H).

***Failure in test 0A indicates a defective RAM.

Test 0B (H) 0000 1011 (B)

DMA controller #1 register check.

Four current address registers (16 bits wide, each) and four current word count registers (16 bits wide, each) for each of the four DMA channels are written to and read from to verify operation.

A failure in test 0B will generate the following display on the console:

"DMA 1 error"

The beeper will sound, and a halt instruction will be executed.

***Failure in test 0B indicates a defective OTI-053, OTI-052.

Test 0C (H) 0000 1100 (B)

DMA controller #2 register check. The second functional 8237 containing four current address registers (16 bits wide, each) and four current word count registers (16 bits wide, each) within the OTI-053, OTI-052 are written to and read from to verify operation.

Successful completion of the test 0C will set the modes for DMA channels 0 through 3 and enable cascading by channels 4, 5 and 6 (DMA 1).

A failure in test 0C will generate the following display on the console:

"DMA 2 error"

The beeper will sound, and a halt instruction will be executed.

***Failure in test 0C indicates a defective OTI-053, OTI-052.

Test 0D (H) 0000 1101 (B)

Interrupt controller #1 test. Patterns are written to, and read from the interrupt mask register (IMR) which controls the interrupt request register (IRR).

A verification is made that no interrupts can occur if "IMR" is set to FF (H). A vector is initialized to a temporary interrupt service routine in the event of a failure.

A test for correct timer 0 interrupt is also made.

A failure in test 0D will generate the following display on the console:

"Interrupt controller 1 error"

The beeper will sound, and a halt instruction will be executed.

***A failure in test 0D indicates a defective OTI-053, OTI-052.

Test 0E (H) 0000 1110 (B)

Interrupt controller #2 test. The second functional 8259 contained in the OTI-053, OTI-052 is tested as in test 0D, without timer test.

A failure in test 0E will generate the following display on the console:

"Interrupt controller 2 error"

The beeper will sound, and a halt instruction will be executed.

***A failure in test 0E indicates a defective OTI-053, OTI-052.

Test 0F (H) 0000 1111 (B)

Check peripheral in/out register. Write and read from PIO register.

A failure in test 0F will generate the following display on the console:

"PIO error"

The beeper will sound, and a halt instruction will be executed.

***A failure in test 0F indicates a defective OTI-053, OTI-052.

Test 10 (H) 0001 0000 (B)

RAM parity test. Blocks of RAM are written to and read from, parity check for odd parity is made. Parity disabled after successful test.

NOTE: C286-LT does not use parity, third parity boards that use parity will enable parity.

"NMI" is enabled and a service routine for a parity error generates the following console message.

"Parity error"

The beeper will sound, and a halt instruction will be executed.

***Failure in test 10 indicates a defective RAM, third party card, NMI, or local bus.

Test 11 (H) 0001 0001 (B)

Test CMOS clock for battery failure and checksum failure.

Beeper will sound if failure is detected. Console will display:

"Battery failure" or "CMOS checksum failure" or both.

***Failure of test 11 indicates a defective battery, or defective oscillator.

Test 12 (H) 0001 0010 (B)

This test is disabled. It is used only in manufacturing tests.

The beeper will sound for a set length prior to the start of test 13 (H). In a system which has passed all tests to this point the beeper sound heard now would be the one heard in the power up routine.

Test 13 (H) 0001 0011 (B)

Setup interrupt controller and move vector tables to RAM. Vector addresses are fetched from top 8K module.

NOTE: Vectors for video were setup in test 09.

Master and slave interrupts are enabled at this point.

Test 13 does not create any error messages.

Test 14 (H) 0001 0100 (B)

Keyboard test. Functional test of the 8242 keyboard controller at U203. A test for a stuck key on keyboard is performed. Check is made to see if key lock is locked.

A failure in test 14 will display the following error message on console:

"Keyboard error"

***Error indicates a defective 8242 controller or a defective keyboard.

Test 15 (H) 0001 0101 (B)

Test and configure the parallel port. Parallel port addresses are setup, reads and writes to ports are done. Set time out.

No error messages are generated by this test.

Test 16 (H) 0001 0110 (B)

Configure serial COM1 and COM2 for OTI-052. Read serial interrupt ID, set number of serial channels.

No error messages are generated by this test.

Test 17 (H) 0001 0111 (B)

Configure memory less than 640K. Parity (for EXPANSION RAM) is enabled.

Memory was tested in test 0A, and "CMOS STATUS" set. A check for a warm boot (ALT/CNTRL/DEL) is made and a comparison of the old and new memory configuration is performed. If a memory size mismatch is detected, the beeper will sound and the following non-fatal error message will be displayed on the console:

"Base memory configuration error"

The new configuration is stored.

***Check the settings for RAM size in the setup utility if you encounter this message.

Test 18 (H) 0001 1000 (B)

Configure memory over 1 megabyte (virtual memory). Check is made on address line 20, a low indicates virtual address mode.

CMOS status is checked as in test 17, a memory size mismatch will sound the beeper and generate the following non-fatal error message on the console:

"Extended memory configuration error"

The new configuration is stored.

***Check the settings for RAM size in the setup utility if you encounter this message.

Test 19 (H) 0001 1001 (B)

Configure keyboard test. Setup keyboard buffers, enable keyboard interrupt and test if key switch is turned to the on position.

If the key switch is off the following message will be displayed on the console:

"Key switch is off. Turn it on to continue."

NOTE: You are in a loop until you turn on the key switch.

Test 1A (H) 0001 1010 (B)

Configure the floppy disk drive. Calculate number of floppy drives present. Check drive type, compare settings stored in CMOS, if a mismatch the following message will be displayed on console:

"Floppy 0 configuration error"

***Check settings in setup utility if above message is displayed.

Test checks second floppy configuration, if a mismatch the following message will be displayed on the console:

"Floppy 1 configuration error"

***Check settings in setup utility if above message is displayed.

New configuration is stored in CMOS. Floppy interrupt is enabled.

Test 1B (H) 0001 1011 (B)

Configure the hard drive. Check configuration if a mismatch hard drive will not be setup.

No error message is generated.

Test 1C (H) 0001 1100 (B)

Test number is not moved to parallel port for this configuration. This routine only turns on the game card bit in the "EQUIP FLAG".

No error message is generated.

Test 1D (H) 0001 1101 (B) — Not valid C286LT

Configure 80287 coprocessor. Check if 80287 is present. Enable 80287 interrupt and set "EQUIP FLAG" if it is.

Compare configuration with CMOS, store new configuration, beep the speaker, and display the following message is setup changed.

"-- Coprocessor (80287) configuration error"

***Check setup utility for correct settings if this message is displayed.

Test 1E (H) 0001 1110 (B)

Check CMOS clock to see if it was initialized and is working. Enable timer interrupt. Sound beeper, and initialize if failure detected, then display one of the following messages on the console:

"-- The Real Time Clock has not been initialized"

OR: "-- Real Time Clock error"

***Check the OTI-054 if second message above is displayed.

Test 1F (H) 0001 1111 (B)

Generate a new CMS checksum and save it in CMOS RAM. Call made to auto configuration program at this point.

No error message generated.

Test 20 (H) Not Implemented

Test 21 (H) 0010 0001 (B)

Initialize ROM drivers, including hard drive. Checksum generated, and all ROMS tested.

System will now begin boot up.

System speed is determined, 6 MHz, 8MHz or 12MHz.

***Refer to operations manual for opening screen display.

Tests 22, 23 Not Implemented

3.7 WIRING DIAGRAM

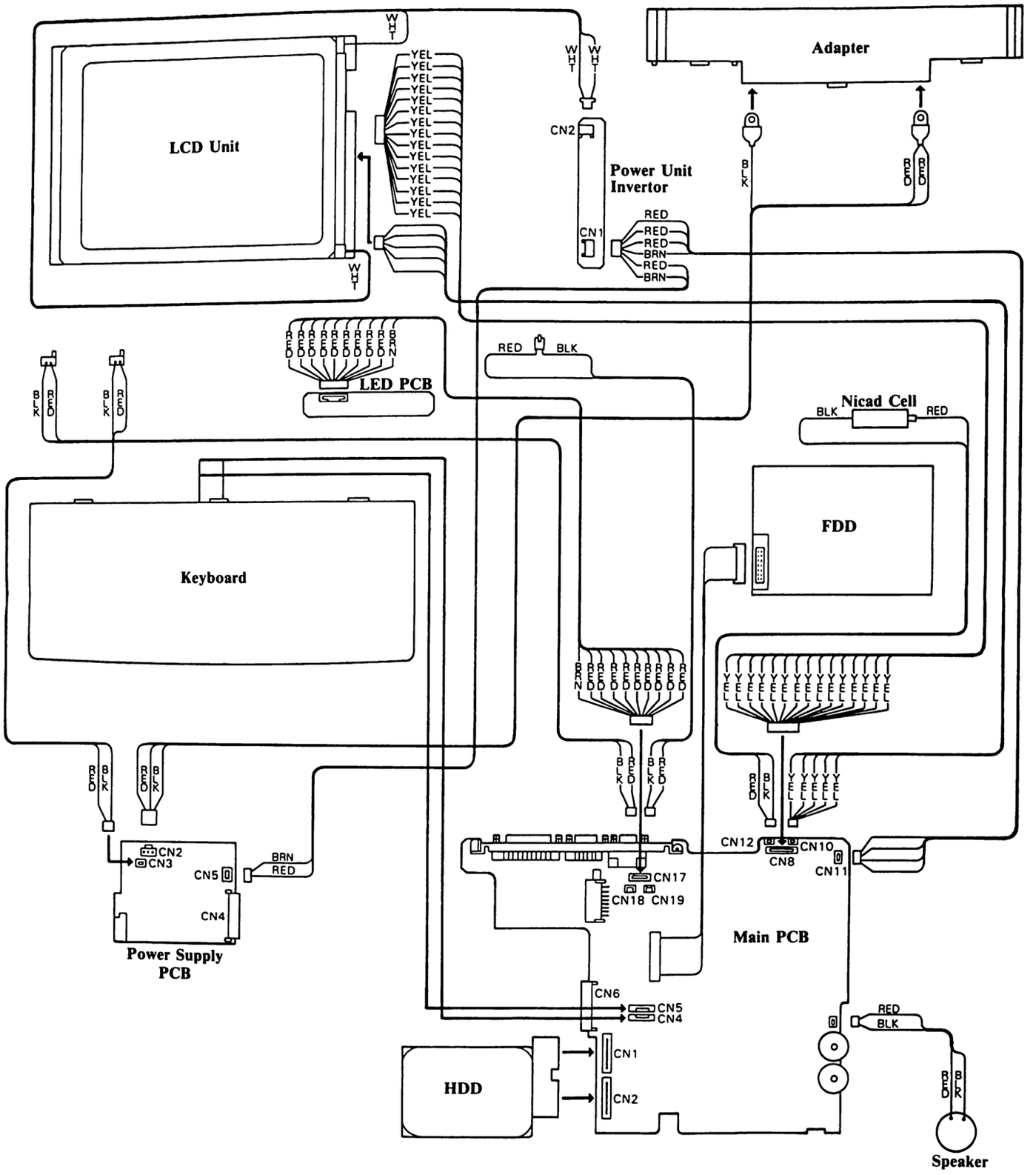


Figure 3.8

Test 24 (H) 0010 0100 (B)

Test operation of the RTC chip. Recheck battery, make sure clock is counting, test memory.

System will execute a halt instruction on memory failure. No error message is generated.

Test 25 (H) 0010 0101 (B)

Used in manufacturing to loop through diagnostics.

Test 26 (H) 0010 0110 (B)

Virutal memory test (over 1 megabyte). Call made to this routine from test 09.

Display Message: "Testing Extended RAM"
Display Message: "Total System RAM = XXXX" at finish.

During this test the exception interrupt vector tables and descriptor tables are built, and moved from ROM to RAM.

A test of address line 20 is made (controls real or virtual CPU mode). If not in virtual mode display following message:

"Test __ 26: Virtual Mode CPU error"

And send F3 (H) (1111 0011 to parallel port. Then execute a halt instruction.

Test address lines 19 through 23 are tested. Shutdown if error. Exception interrupt codes are moved to the parallel port prior to shutdown. The following list defines the code sent to the port and the type of exception interupt (EXECP INT).

81	(H)	EXECP INT 01	Single Step
82	(H)	EXECP INT 02	NMI
83	(H)	EXECP INT 03	Breakpoint
84	(H)	EXECP INT 04	Into Detect
85	(H)	EXECP INT 05	Boundary
86	(H)	EXECP INT 06	Invalid OP Code
87	(H)	EXECP INT 07	—
88	(H)	EXECP INT 08	Double Exception
89	(H)	EXECP INT 09	Processor Segment Error
8A	(H)	EXECP INT 10	—
8B	(H)	EXECP INT 11	Segment Not Present
8C	(H)	EXECP INT 12	Stack Segment Not Present
8D	(H)	EXECP INT 13	General Protection Error
8E	(H)	EXECP INT 14	—
8F	(H)	EXECP INT 15	—
90	(H)	EXECP INT 16	Processor Extension Error

Power on diagnostic program is finished at the time of boot up (end of test 21).

Note that during execution of "POD" calls are made to auto configure and to miscellaneous interrupt routines.

All error messages listed in appendix L of operations guide are listed in the overview above with the exception of the following which are generated from the miscellaneous interrupt routines.

10 "Parity error on main circuit board"

11 "Parity error on expansion bus"

12 "Non-recoverable error - Processor halted"

13 "Press F1 key to continue"

Messages 10, 11 are generated after a parity error has been detected and a memory check has determined that it was on the main board, or the expansion bus. If the check finds the error the CPU is halted and message 12 is displayed. If no error is found after the check, message 13 is displayed and processing will continue.

SECTION 4

PARTS

COMMODORE STOCKED PARTS
C286-LT MAJOR ASSEMBLIES — FIELD REPLACEMENT UNITS (FRU)

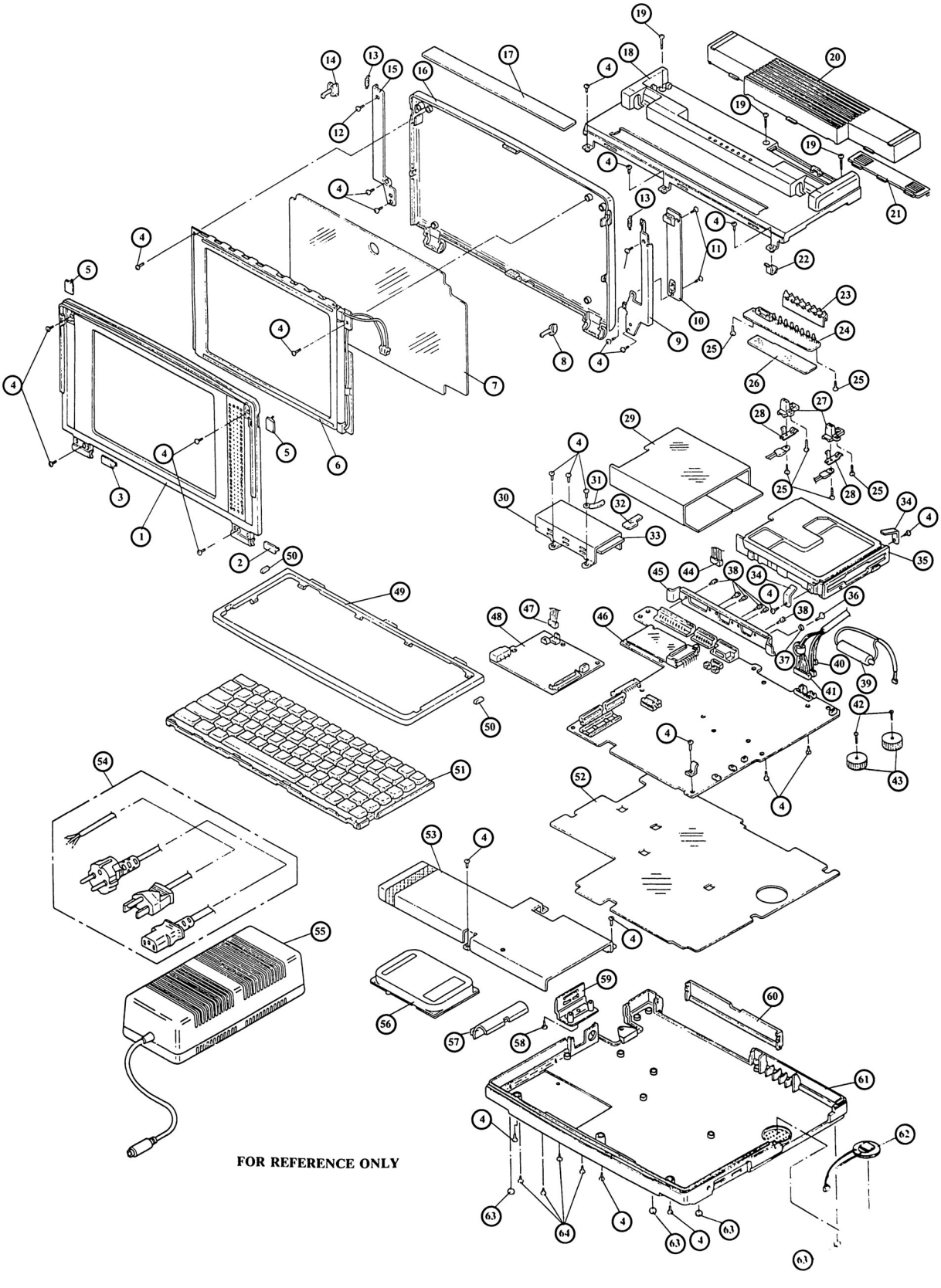
390774-01	AC Power Adapter
903508-15	Power Cord, Shielded
390790-01	Battery Pack
312569-01	Carrying Bag
390840-01	Door — Rear Panel
390839-01	Bezel — Modem (Cover)
363559-01	LCD Display Assembly
363554-01	Keyboard Assembly
390841-01	Lithium Cell
363553-01	PCB Assembly — Power SR170
400500-01*	PCB Main Assembly
312897-01	Drive Assembly — 3.5 Floppy
390843-01	Cable — Floppy Drive
312896-01	Drive Assembly — 20MB Hard Drive
394018-01	Cable — Hard Drive
315984-01	Software Sub Assembly
363573-01**	Manual, Operations Guide

*Number silk screened on PCB is not the Commodore part number for spare part.

**Operations guide is included in software sub assembly.

SERVICE REFERENCE PARTS DIAGRAM

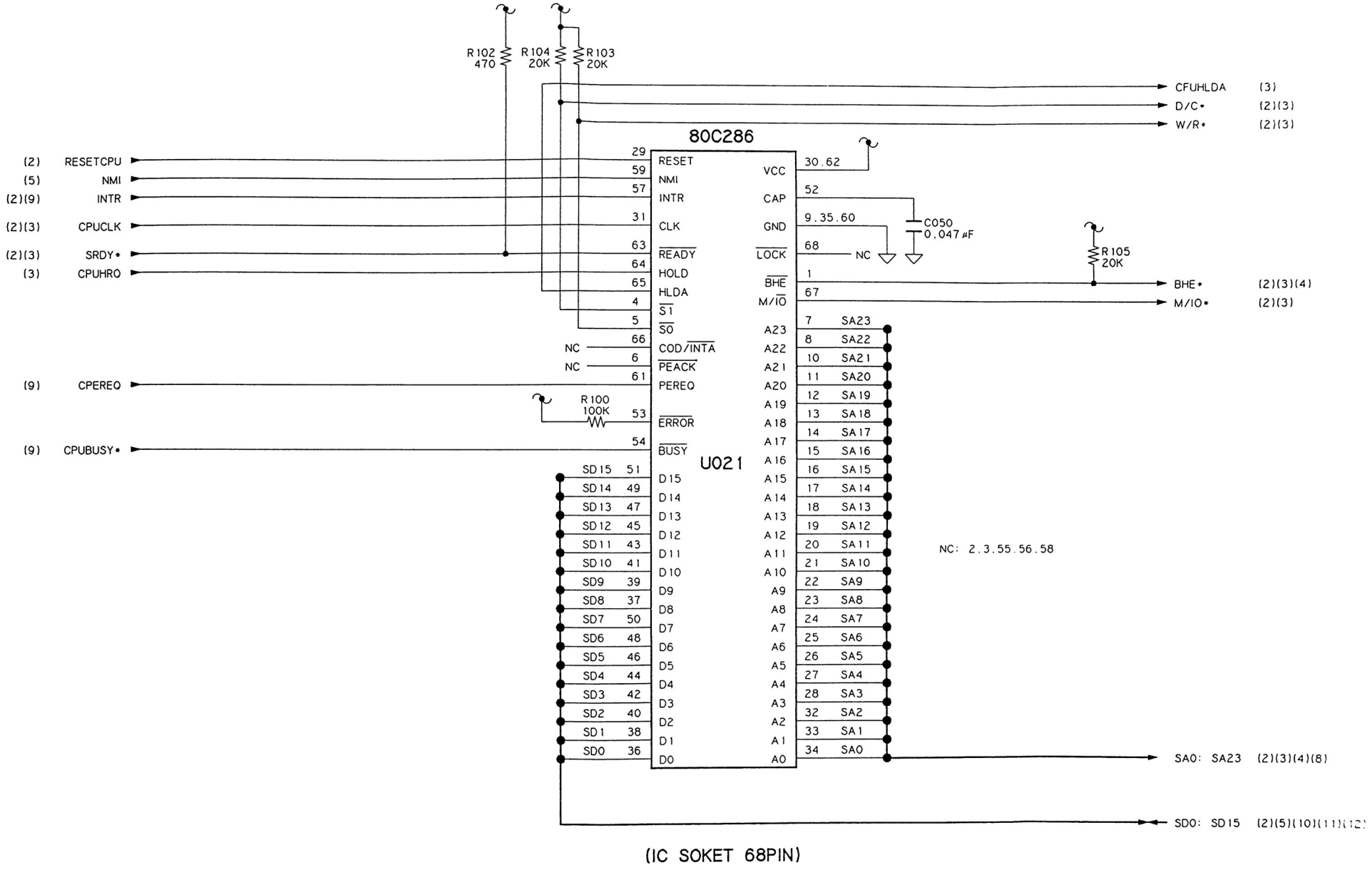
DESCRIPTION	REF. #	DESCRIPTION	REF. #	DESCRIPTION	REF. #	DESCRIPTION	REF. #
Mask LCD	1	Function Sheet	17	Insulator Case Modem	33	Top Cabinet Front	49
Cover Screw Hinge Right	2	Top Cabinet Rear	18	Plate Spring	34	Damper LCD (x2)	50
Cover Screw Hinge Left	3	SCR Bin 3x25 (x3)	19	Floppy Disk Drive	35	Keyboard	51
SCR Bin 3x6 (x26)	4	Nicad Cell 10KR-1700AE-C	20	SCR Bin 4x6	36	Insulator PCB	52
Cover Screw LCD (x2)	5	Cover Assy. (Battery)	21	Washer Out TW 4	37	Shield HDD	53
LCD LCM-5630	6	Plate Spring	22	Screw Holder-PFB (x6)	38	AC Cord-Pea	54
Insulator LCD	7	Glass LED	23	Lithium Cell MBC1	39	AC Adaptor/Quick Charger	55
Stopper LCD Right	8	Pw Board Assy Note LED Cl	24	Connecting Cable LCD-PS	40	Hard Disk Drive	56
Bracket LCD Right	9	SCR S-TPG BRZ 2.6x12 (x6)	25	Connecting Cable LCD-SIG	41	Connecting Cable HDD	57
Power Unit Invertor	10	Insulator LED PCB	26	SCR Pan Head 1.4x4 (x2)	42	SCR Bin 3x6	58
SCR Bin 2.6x5 (x2)	11	Holder Contact (x2)	27	Knob Volume (x2)	43	Bezel Modem	59
SCR S-TPG Bin 3x8 (x2)	12	Contact (x2)	28	Connecting Cable LED	44	Door	60
Extension Spring (x2)	13	Insulator FDD	29	Rear Panel	45	Bottom Cabinet	61
Stopper LCD Left	14	Case Modem	30	Pw Board Assy Note Main	46	Speaker TS30R-8B3A-B	62
Bracket LCD Left	15	Cable Clamp-LBA	31	Connecting Cable Assy 3P	47	Foot (x4)	63
Cabinet LCD	16	Insulator Contact	32	Pw Board Assy SR170	48	Special Screw (x4)	64

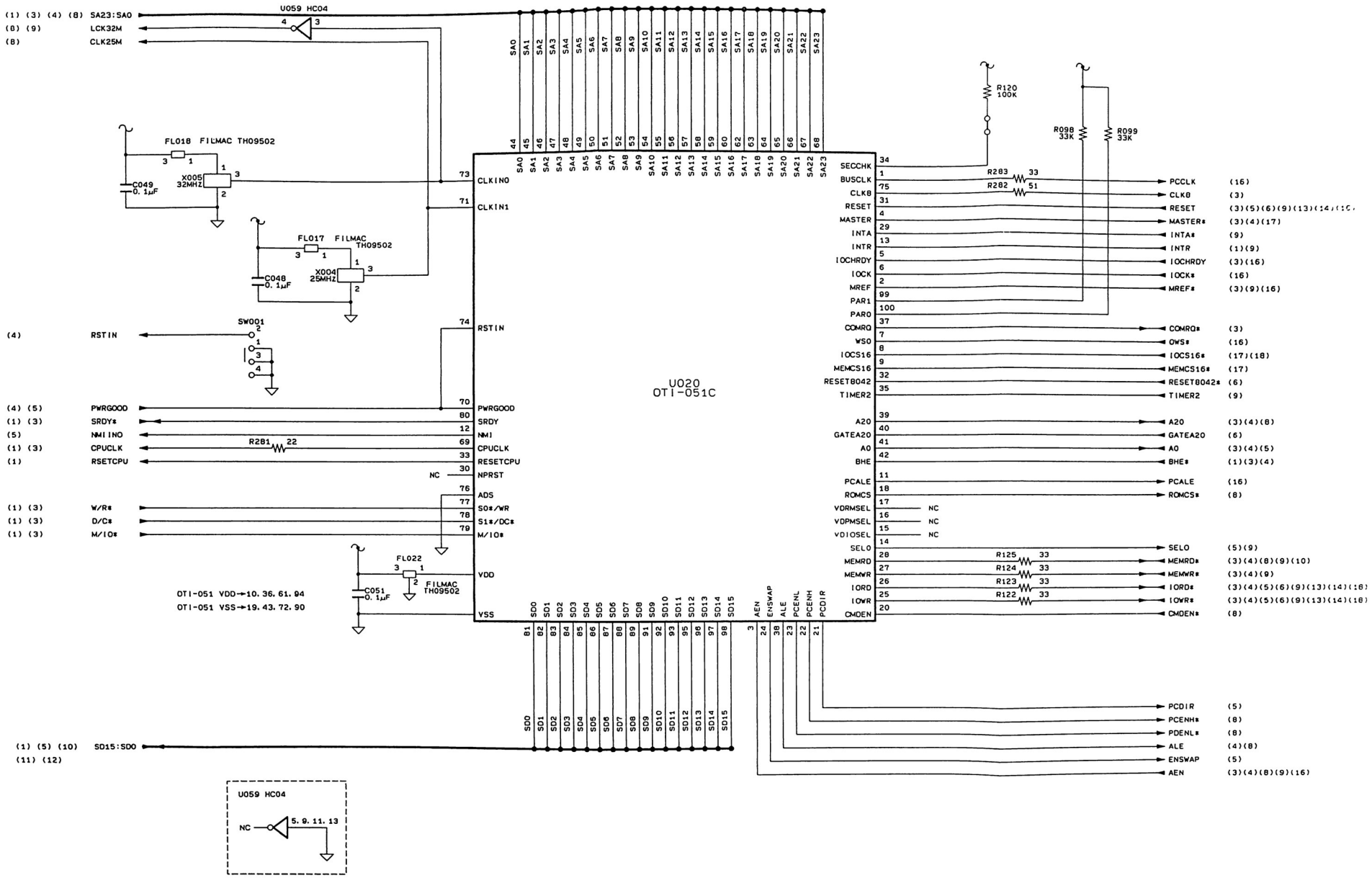


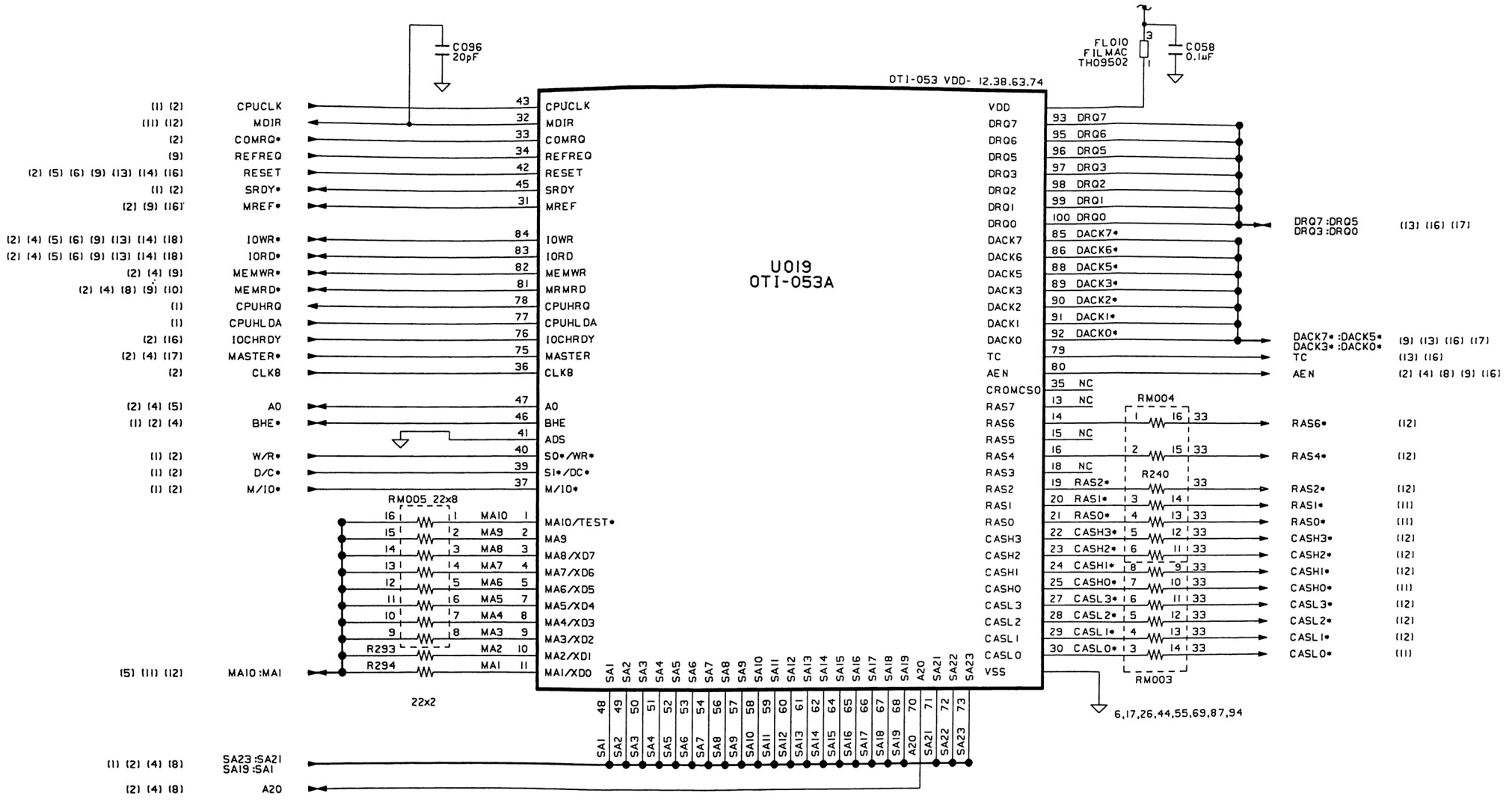
FOR REFERENCE ONLY

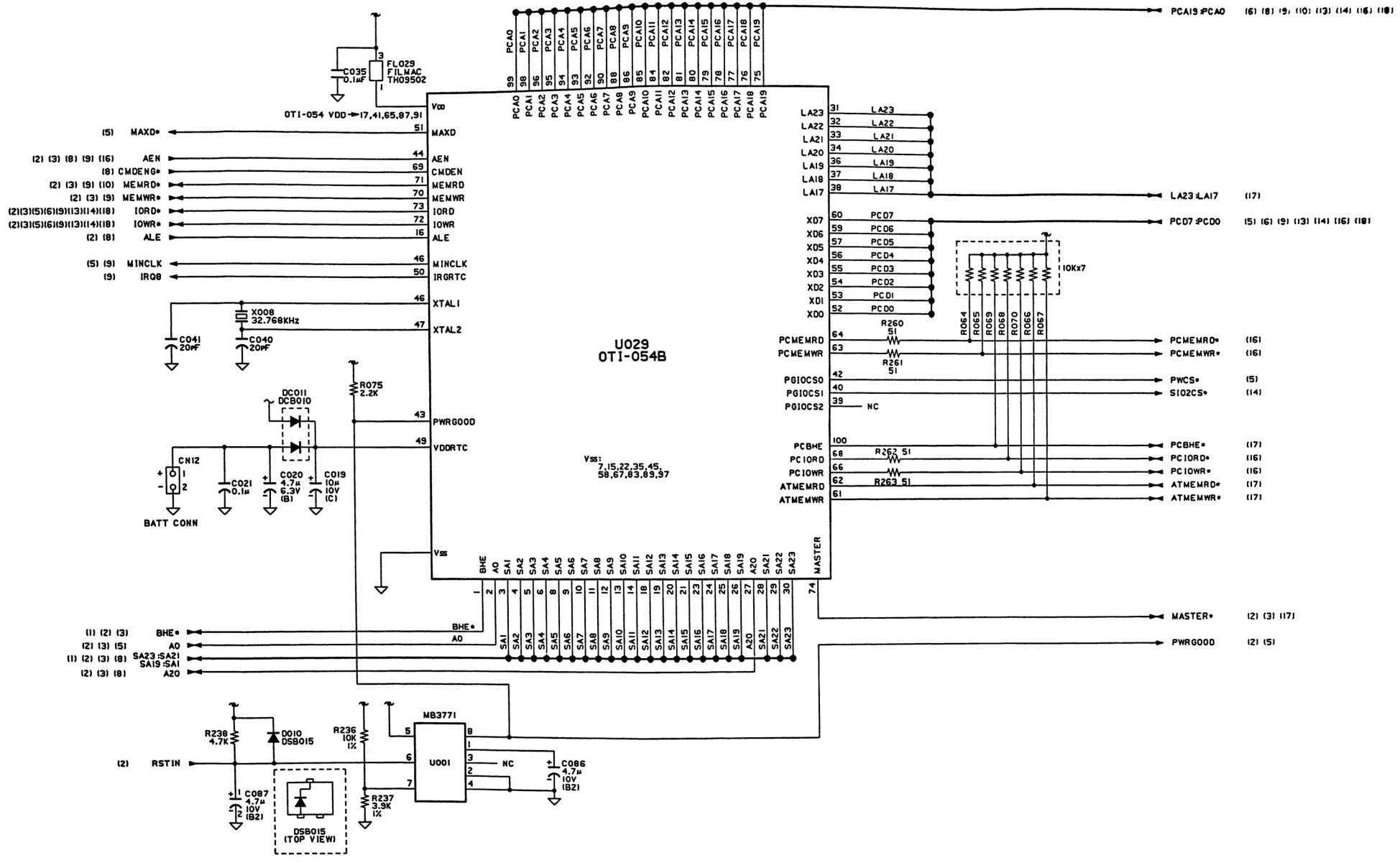
SECTION 5

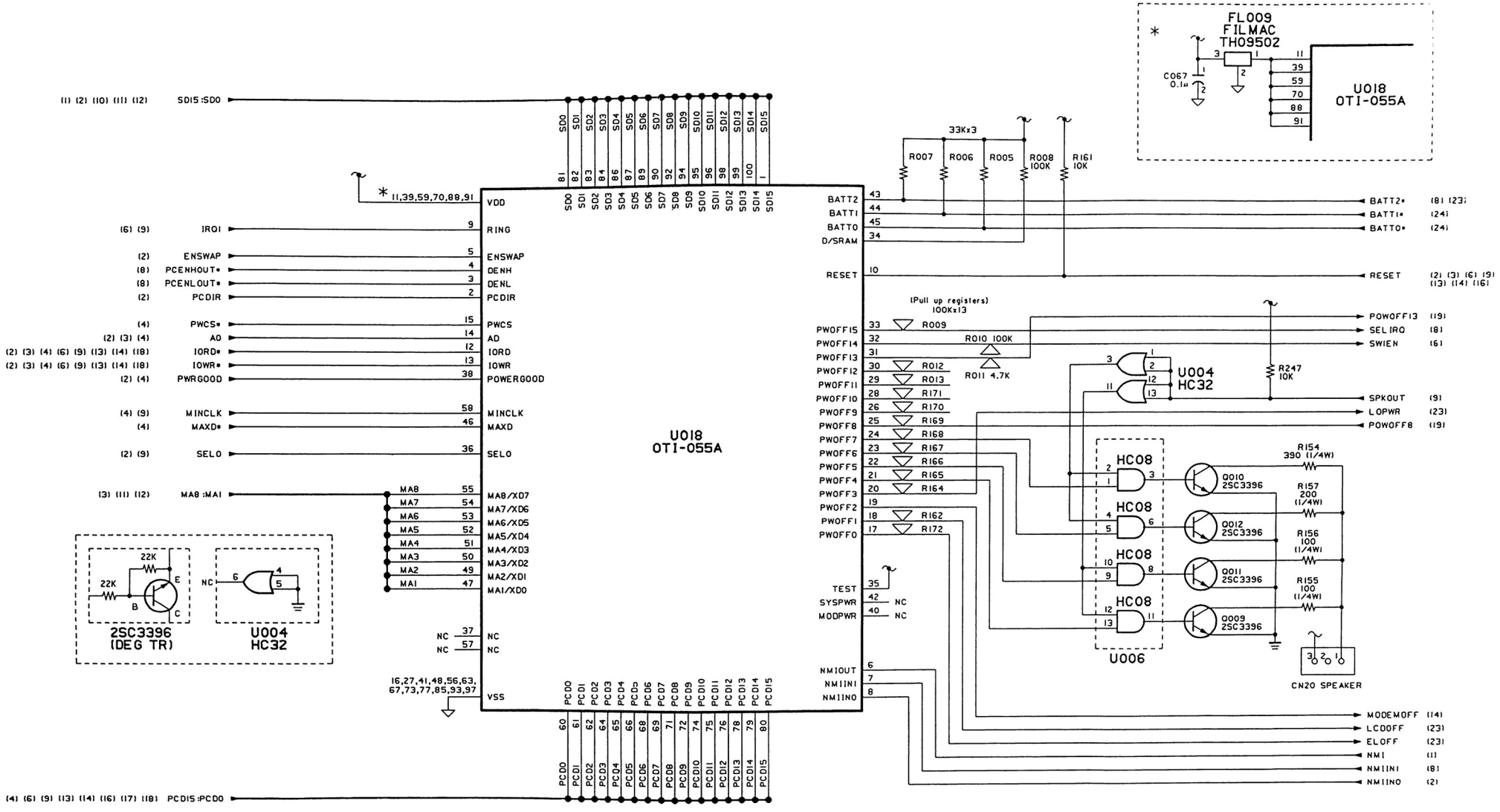
SCHEMATICS

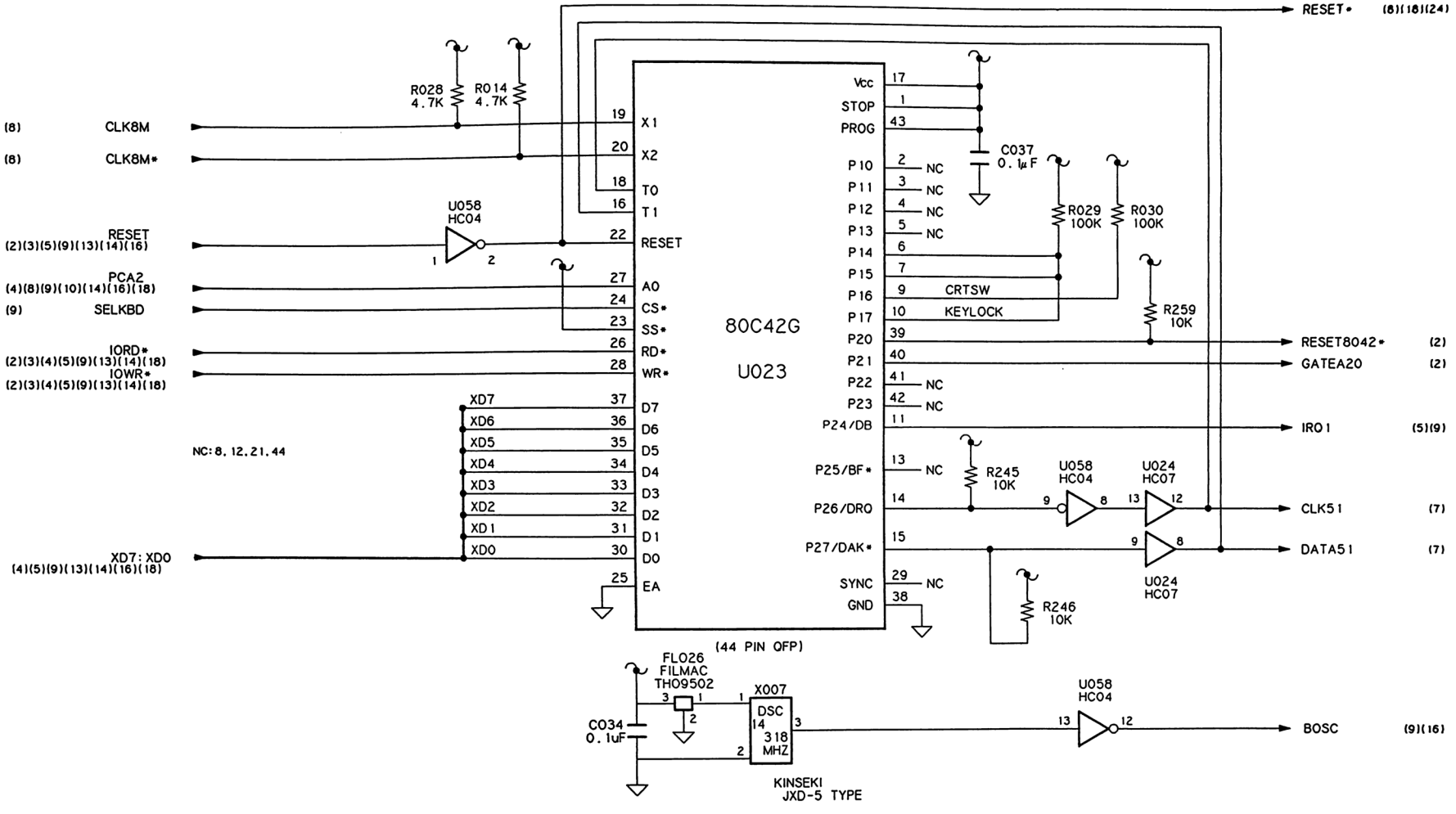

R102 470
R104 20K
R103 20K
80C286
U021
(2) RESETCPU
(5) NMI
(2)(9) INTR
(2)(3) CPUCLK
(2)(3) SRDY*
(3) CPUHRQ
(9) CPEREQ
(9) CPUBUSY*
R100 100K
CFUHLDA (3)
D/C* (2)(3)
W/R* (2)(3)
30.62
52
9.35.60
C050 0.047 µF
68 NC
R105 20K
BHE* (2)(3)(4)
M/IO* (2)(3)
NC: 2.3.55.56.58
SA0: SA23 (2)(3)(4)(8)
SD0: SD15 (2)(5)(10)(11)(12)
(IC SOKET 68PIN)

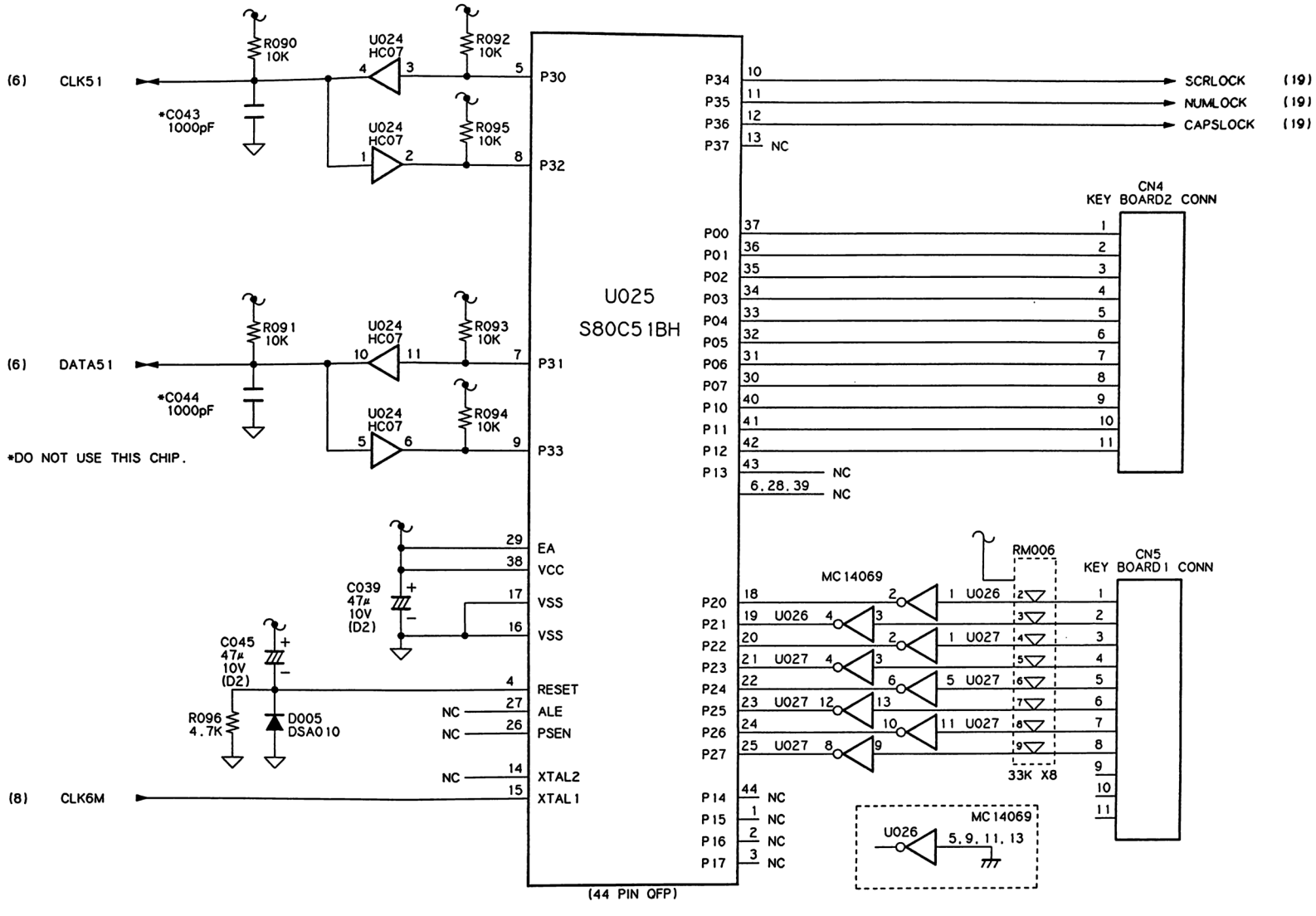

U059 HC04
(1) (3) (4) (8) SA23:SA0
(8) (9) LCK32M
(8) CLK25M
FL018 FILMAC TH09502
X005 32MHZ
C049 0.1µF
FL017 FILMAC TH09502
X004 25MHZ
C048 0.1µF
SW001
(4) RSTIN
(4) (5) PWRGOOD
(1) (3) SRDY#
(5) NMIINO
(1) (3) CPUCLK
(1) RSETCPU
R281 22
(1) (3) W/R#
(1) (3) D/C#
(1) (3) M/IO#
FL022
FILMAC TH09502
C051 0.1µF
OTI-051 VDD→10. 36. 61. 94
OTI-051 VSS→19. 43. 72. 90
U020
OTI-051C
CLKIN0
CLKIN1
RSTIN
PWRGOOD
SRDY
NMI
CPUCLK
RESETCPU
NPRST
ADS
S0#/WR
S1#/DC#
M/IO#
VDD
VSS
R120 100K
R098 33K
R099 33K
R283 33
R282 51
R125 33
R124 33
R123 33
R122 33
(1) (5) (10) (11) (12) SD15:SD0
U059 HC04
NC
5. 9. 11. 13

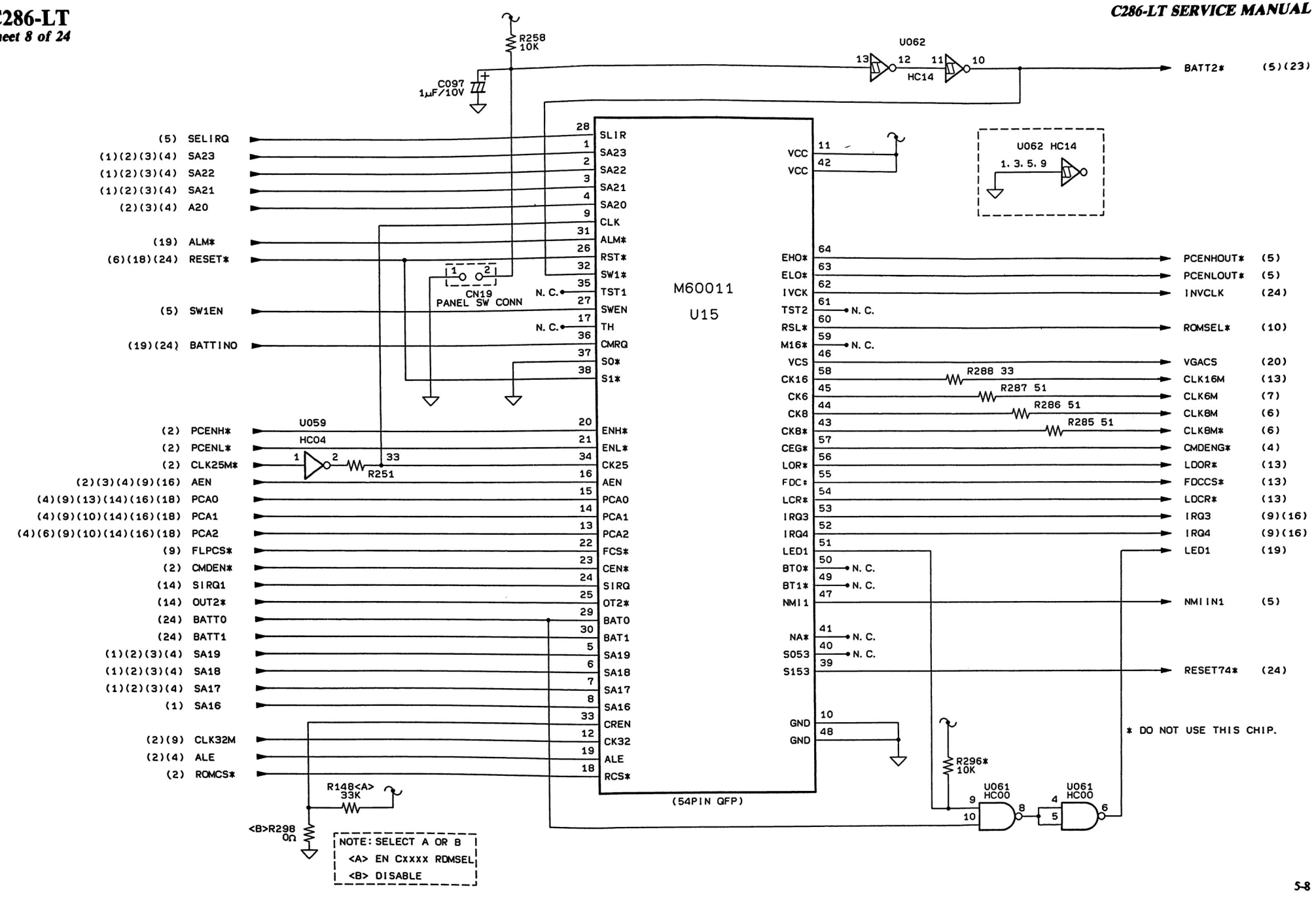

C096
20pF
FL010
FILMAC
TH09502
C058
0.1uF
OTI-053 VDD- 12.38.63.74
U019
OTI-053A
CPUCLK
MDIR
COMRQ
REFREQ
RESET
SRDY
MREF
IOWR
IORD
MEMWR
MRMRD
CPUHRQ
CPUHLDA
IOCHRDY
MASTER
CLK8
A0
BHE
ADS
S0*/WR*
S1*/DC*
M/IO*
MA10/TEST*
MA9
MA8/XD7
MA7/XD6
MA6/XD5
MA5/XD4
MA4/XD3
MA3/XD2
MA2/XD1
MA1/XD0
VDD
DRQ7
DRQ6
DRQ5
DRQ3
DRQ2
DRQ1
DRQ0
DACK7
DACK6
DACK5
DACK3
DACK2
DACK1
DACK0
TC
AEN
CROMCS0
RAS7
RAS6
RAS5
RAS4
RAS3
RAS2
RAS1
RAS0
CASH3
CASH2
CASH1
CASH0
CASL3
CASL2
CASL1
CASL0
VSS
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
A20
SA21
SA22
SA23
RM005 22x8
R293
R294
22x2
RM004
R240
RM003
DRQ7:DRQ5
DRQ3:DRQ0
DACK7*:DACK5*
DACK3*:DACK0*
TC
AEN
RAS6*
RAS4*
RAS2*
RAS1*
RAS0*
CASH3*
CASH2*
CASH1*
CASH0*
CASL3*
CASL2*
CASL1*
CASL0*
6,17,26,44,55,69,87,94
MA10:MA1
SA23:SA21
SA19:SA1
A20

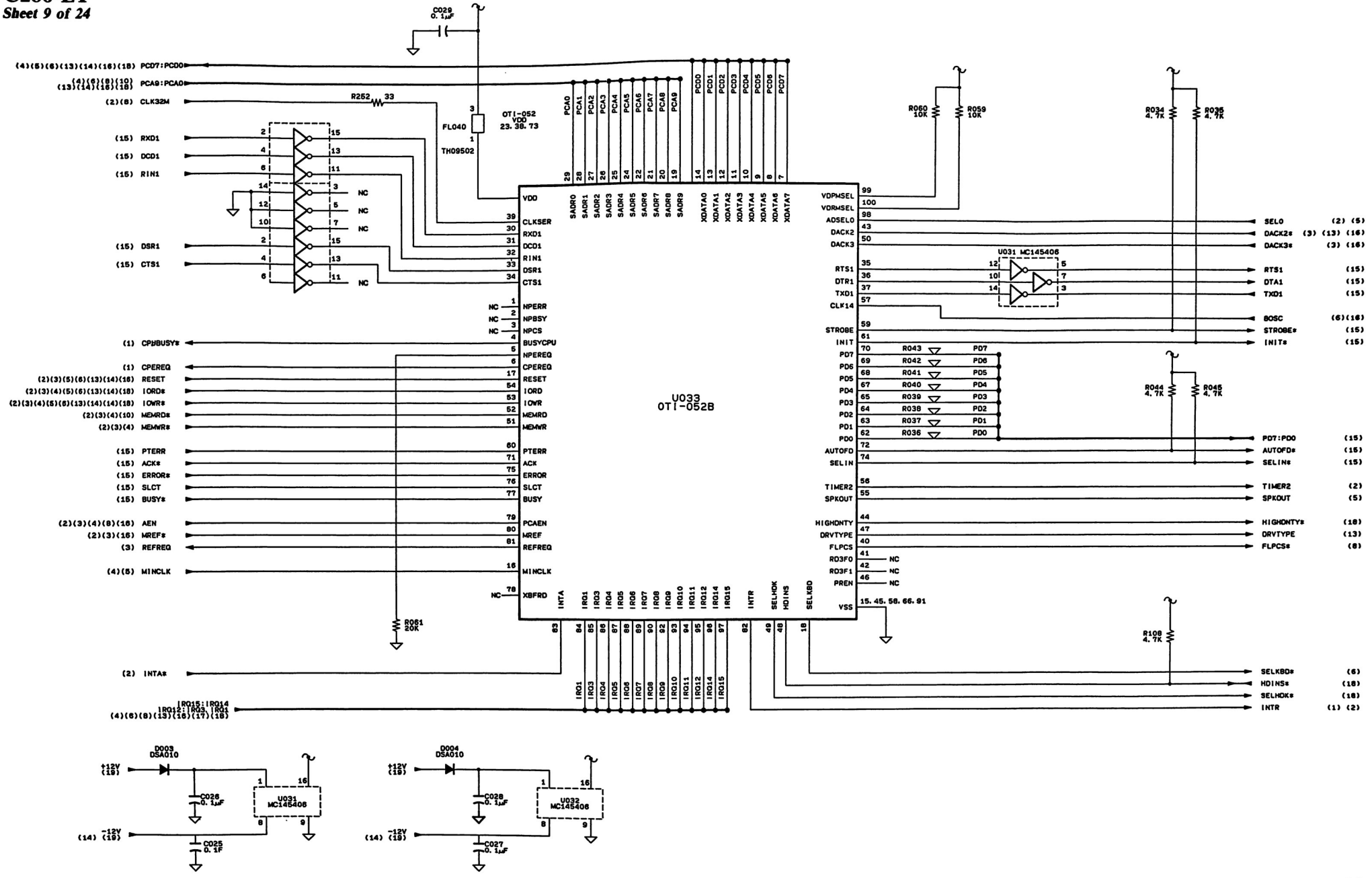

U029
0TI-054B
0TI-054 VDD ►17,41,65,87,91
Vss:
7,15,22,35,45,
58,67,83,89,97
FL029
FILMAC
TH09502
C035
0.1µF
X008
32.768KHz
C041
20PF
C040
20PF
R075
2.2K
DC011
DCB010
CN12
BATT CONN
C021
0.1µ
C020
4.7µ
6.3V
(B)
C019
10µ
10V
(C)
R260
51
R261
51
R262 51
R263 51
10Kx7
R064
R065
R069
R068
R070
R066
R067
MB3771
U001
R238
4.7K
DO10
DSB015
R236
10K
1%
R237
3.9K
1%
C086
4.7µ
10V
(B2)
C087
4.7µ
10V
(B2)
DSB015
(TOP VIEW)
MAXD*
AEN
CMDENG*
MEMRD*
MEMWR*
IORD*
IOWR*
ALE
MINCLK
IRQ8
XTAL1
XTAL2
PWRGOOD
VDDRTC
Vss
BHE*
A0
SA23:SA21
SA19:SA1
A20
RSTIN
NC
PCMEMRD
PCMEMWR
PCIOCS0
PCIOCS1
PCIOCS2
PCBHE*
PCIORD*
PCIOWR*
ATMEMRD*
ATMEMWR*
MASTER
PCA19:PCA0
LA23:LA17
PCD7:PCD0
PWCS*
SIO2CS*
MASTER*

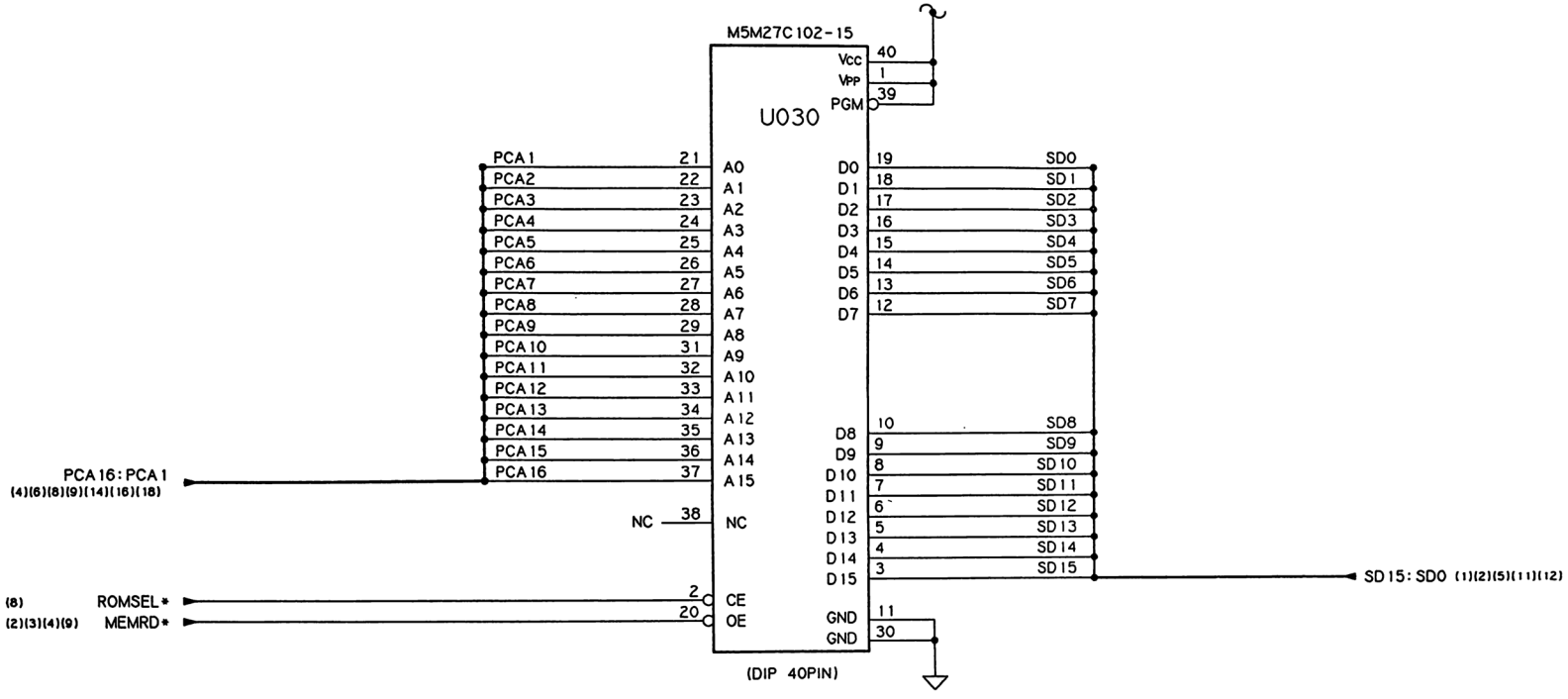

U018
OTI-055A
FL009
FILMAC
TH09502
C067
0.1µ
33Kx3
R007
R006
R005
R008
100K
R161
10K
(Pull up registers)
100Kx13
R009
R010 100K
R011 4.7K
R012
R013
R171
R170
R169
R168
R167
R166
R165
R164
R162
R172
R247
10K
U004
HC32
HC08
U006
Q010
2SC3396
Q012
2SC3396
Q011
2SC3396
Q009
2SC3396
R154
390 (1/4W)
R157
200
(1/4W)
R156
100
(1/4W)
R155
100
(1/4W)
CN20 SPEAKER
22K
22K
2SC3396
(DEG TR)
U004
HC32
SDI5:SD0
PCDI5:PCD0
MA8:MA1
IROI
ENSWAP
PCENHOUT*
PCENLOUT*
PCDIR
PWCS*
A0
IORD*
IOWR*
PWRGOOD
MINCLK
MAXD*
SEL0
BATT2
BATT1
BATT0
D/SRAM
RESET
TEST
SYSPWR
MODPWR
NMIOUT
NMIIN1
NMIIN0
PWOFF15
PWOFF14
PWOFF13
PWOFF12
PWOFF11
PWOFF10
PWOFF9
PWOFF8
PWOFF7
PWOFF6
PWOFF5
PWOFF4
PWOFF3
PWOFF2
PWOFF1
PWOFF0
POWOFF13
SELIRQ
SWIEN
SPKOUT
LOPWR
POWOFF8
MODEMOFF
LCDOFF
ELOFF
NMI
NMIIN1
NMIIN0

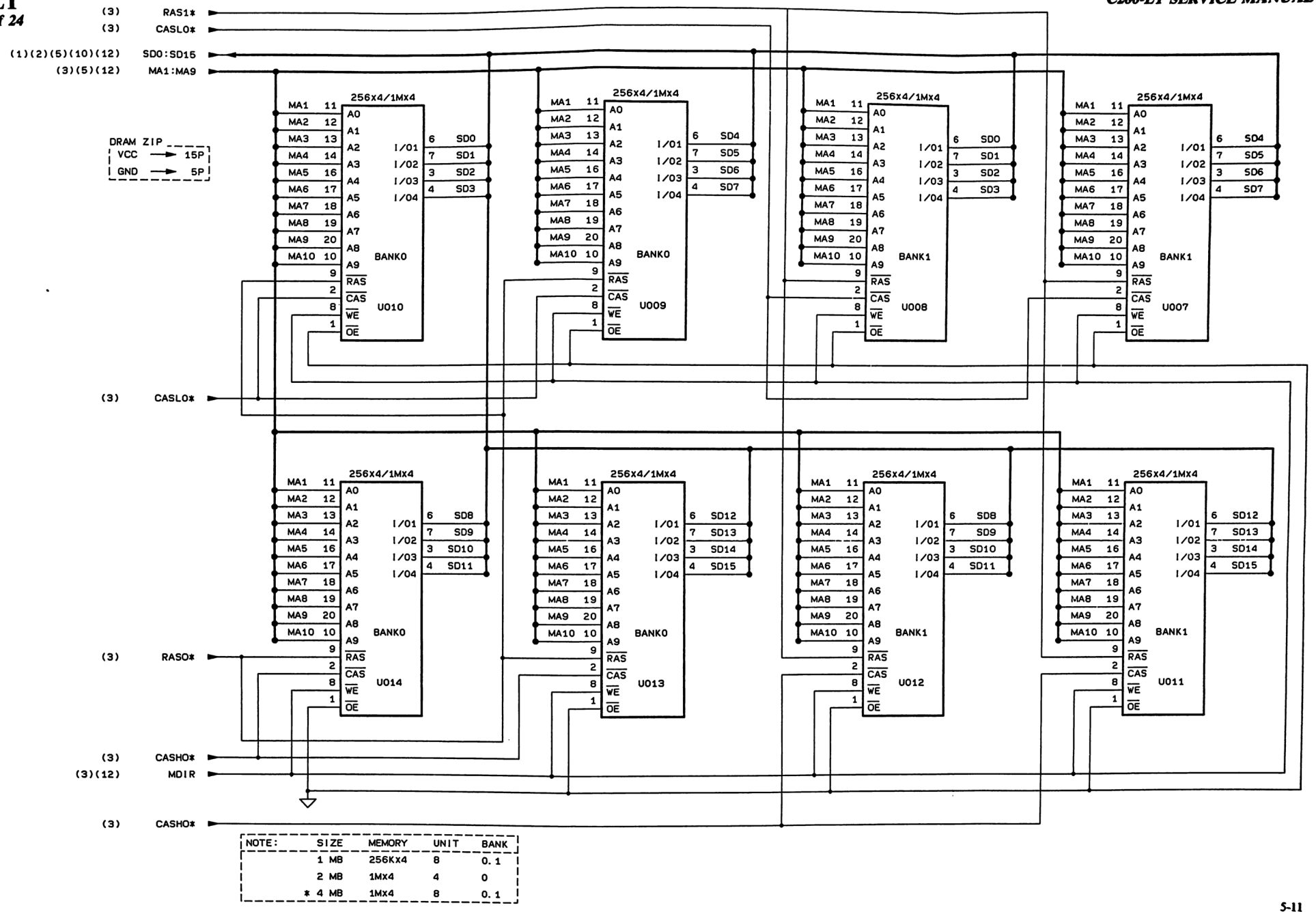

RESET* (8)(18)(24)
R028 4.7K
R014 4.7K
(8) CLK8M
(8) CLK8M*
U058 HC04
RESET (2)(3)(5)(9)(13)(14)(16)
PCA2 (4)(8)(9)(10)(14)(16)(18)
(9) SELKBD
IORD* (2)(3)(4)(5)(9)(13)(14)(18)
IOWR* (2)(3)(4)(5)(9)(13)(14)(18)
NC: 8, 12, 21, 44
XD7: XD0 (4)(5)(9)(13)(14)(16)(18)
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XD0
19 X1
20 X2
18 T0
16 T1
22 RESET
27 A0
24 CS*
23 SS*
26 RD*
28 WR*
37 D7
36 D6
35 D5
34 D4
33 D3
32 D2
31 D1
30 D0
25 EA
80C42G
U023
(44 PIN QFP)
Vcc 17
STOP 1
PROG 43
C037 0.1μF
P10 2 NC
P11 3 NC
P12 4 NC
P13 5 NC
P14 6
P15 7
P16 9 CRTSW
P17 10 KEYLOCK
R029 100K
R030 100K
R259 10K
P20 39
P21 40
P22 41 NC
P23 42 NC
P24/DB 11
P25/BF* 13 NC
P26/DRQ 14
P27/DAK* 15
SYNC 29 NC
GND 38
R245 10K
R246 10K
U058 HC04
U024 HC07
U024 HC07
RESET8042* (2)
GATEA20 (2)
IRQ1 (5)(9)
CLK51 (7)
DATA51 (7)
FL026 FILMAC TH09502
X007 DSC 14 3.18 MHZ
C034 0.1uF
KINSEKI JXD-5 TYPE
U058 HC04
BOSC (9)(16)


(6) CLK51
*C043 1000pF
R090 10K
U024 HC07
R092 10K
U024 HC07
R095 10K
P30
P32
(6) DATA51
*C044 1000pF
R091 10K
U024 HC07
R093 10K
U024 HC07
R094 10K
P31
P33
*DO NOT USE THIS CHIP.
C039 47µ 10V (D2)
C045 47µ 10V (D2)
R096 4.7K
D005 DSA010
(8) CLK6M
EA
VCC
VSS
VSS
RESET
ALE
PSEN
XTAL2
XTAL1
U025
S80C51BH
(44 PIN QFP)
P34
P35
P36
P37
P00
P01
P02
P03
P04
P05
P06
P07
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21
P22
P23
P24
P25
P26
P27
NC
SCRLOCK (19)
NUMLOCK (19)
CAPSLOCK (19)
CN4
KEY BOARD2 CONN
CN5
KEY BOARD1 CONN
RM006
33K X8
MC14069
U026
U027
MC14069
U026
5, 9, 11, 13

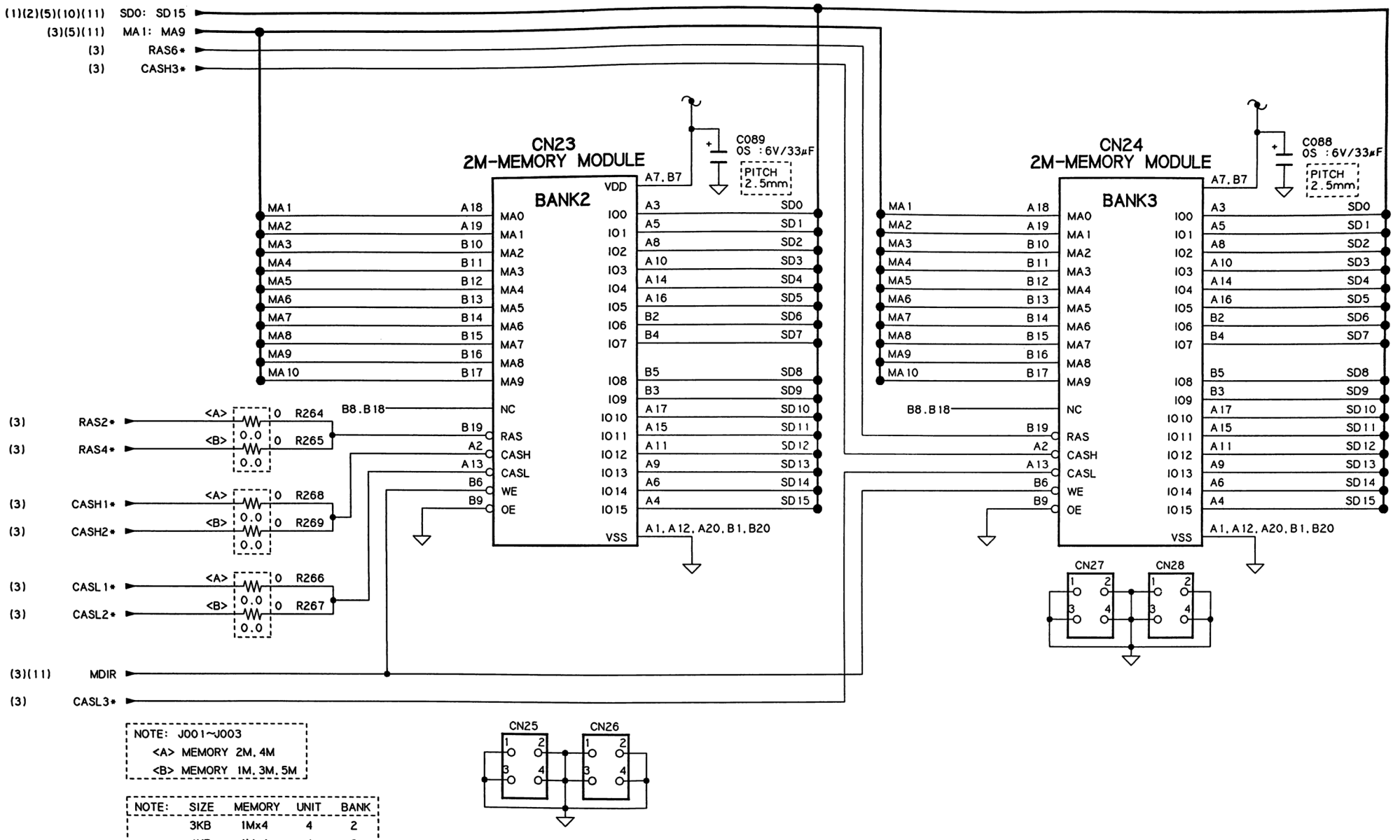

R258
10K
C097
1µF/10V
U062
HC14
BATT2* (5)(23)
(5) SELIRQ
(1)(2)(3)(4) SA23
(1)(2)(3)(4) SA22
(1)(2)(3)(4) SA21
(2)(3)(4) A20
(19) ALM*
(6)(18)(24) RESET*
(5) SW1EN
(19)(24) BATTINO
CN19
PANEL SW CONN
N. C.
M60011
U15
SLIR
SA23
SA22
SA21
SA20
CLK
ALM*
RST*
SW1*
TST1
SWEN
TH
CMRQ
S0*
S1*
VCC
VCC
U062 HC14
1. 3. 5. 9
EHO*
ELO*
IVCK
TST2
RSL*
M16*
VCS
CK16
CK6
CK8
CK8*
CEG*
LOR*
FDC*
LCR*
IRQ3
IRQ4
LED1
BT0*
BT1*
NMI1
NA*
S053
S153
GND
GND
PCENHOUT* (5)
PCENLOUT* (5)
INVCLK (24)
ROMSEL* (10)
VGACS (20)
CLK16M (13)
CLK6M (7)
CLK8M (6)
CLK8M* (6)
CMDENG* (4)
LDOR* (13)
FDCCS* (13)
LDCR* (13)
IRQ3 (9)(16)
IRQ4 (9)(16)
LED1 (19)
NMI IN1 (5)
RESET74* (24)
R288 33
R287 51
R286 51
R285 51
U059
HC04
R251
(2) PCENH*
(2) PCENL*
(2) CLK25M*
(2)(3)(4)(9)(16) AEN
(4)(9)(13)(14)(16)(18) PCA0
(4)(9)(10)(14)(16)(18) PCA1
(4)(6)(9)(10)(14)(16)(18) PCA2
(9) FLPCS*
(2) CMDEN*
(14) SIRQ1
(14) OUT2*
(24) BATT0
(24) BATT1
(1)(2)(3)(4) SA19
(1)(2)(3)(4) SA18
(1)(2)(3)(4) SA17
(1) SA16
(2)(9) CLK32M
(2)(4) ALE
(2) ROMCS*
ENH*
ENL*
CK25
AEN
PCA0
PCA1
PCA2
FCS*
CEN*
SIRQ
OT2*
BAT0
BAT1
SA19
SA18
SA17
SA16
CREN
CK32
ALE
RCS*
(54PIN QFP)
R148<A>
33K
<B>R298
0Ω
R296*
10K
U061
HC00
U061
HC00
* DO NOT USE THIS CHIP.
NOTE: SELECT A OR B
<A> EN Cxxxx RDMSEL
<B> DISABLE


U033
0TI-052B
C029
0.1μF
FL040
TH09502
OTI-052
VDD
23.38.73
R252
33
R060
10K
R059
10K
R034
4.7K
R035
4.7K
R044
4.7K
R045
4.7K
R061
20K
R108
4.7K
U031 MC145406
U031
MC145406
U032
MC145406
C026
0.1μF
C025
0.1F
C028
0.1μF
C027
0.1μF
D003
DSA010
D004
DSA010
+12V
-12V
PCD7:PCD0
PCA9:PCA0
CLK32M
RXD1
DCD1
RIN1
DSR1
CTS1
CPUBUSY*
CPEREQ
RESET
IORD*
IOWR*
MEMRD*
MEMWR*
PTERR
ACK*
ERROR*
SLCT
BUSY*
AEN
MREF*
REFREQ
MINCLK
INTA*
IRQ15:IRQ14
IRQ12:IRQ03, IRQ01
SEL0
DACK2*
DACK3*
RTS1
DTA1
TXD1
BOSC
STROBE*
INIT*
PD7:PD0
AUTOFD*
SELIN*
TIMER2
SPKOUT
HIGHDNTY*
DRVTYPE
FLPCS*
SELKBD*
HDINS*
SELHDK*
INTR


M5M27C102-15
U030
Vcc 40
VPP 1
PGM 39
PCA1 21 A0
PCA2 22 A1
PCA3 23 A2
PCA4 24 A3
PCA5 25 A4
PCA6 26 A5
PCA7 27 A6
PCA8 28 A7
PCA9 29 A8
PCA10 31 A9
PCA11 32 A10
PCA12 33 A11
PCA13 34 A12
PCA14 35 A13
PCA15 36 A14
PCA16 37 A15
PCA16:PCA1
(4)(6)(8)(9)(14)(16)(18)
NC 38 NC
(8) ROMSEL* 2 CE
(2)(3)(4)(9) MEMRD* 20 OE
D0 19 SD0
D1 18 SD1
D2 17 SD2
D3 16 SD3
D4 15 SD4
D5 14 SD5
D6 13 SD6
D7 12 SD7
D8 10 SD8
D9 9 SD9
D10 8 SD10
D11 7 SD11
D12 6 SD12
D13 5 SD13
D14 4 SD14
D15 3 SD15
SD15:SD0 (1)(2)(5)(11)(12)
GND 11
GND 30
(DIP 40PIN)

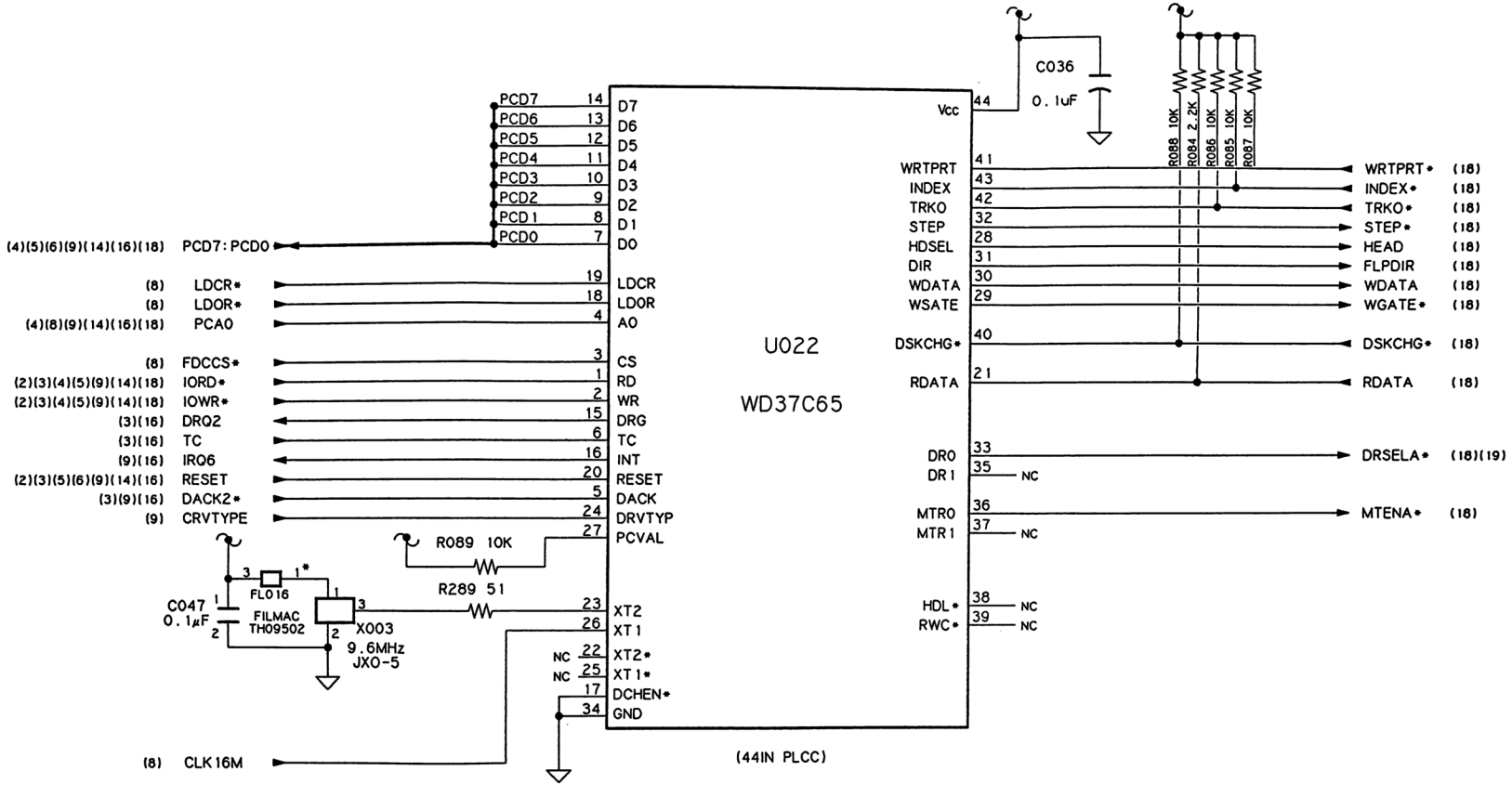


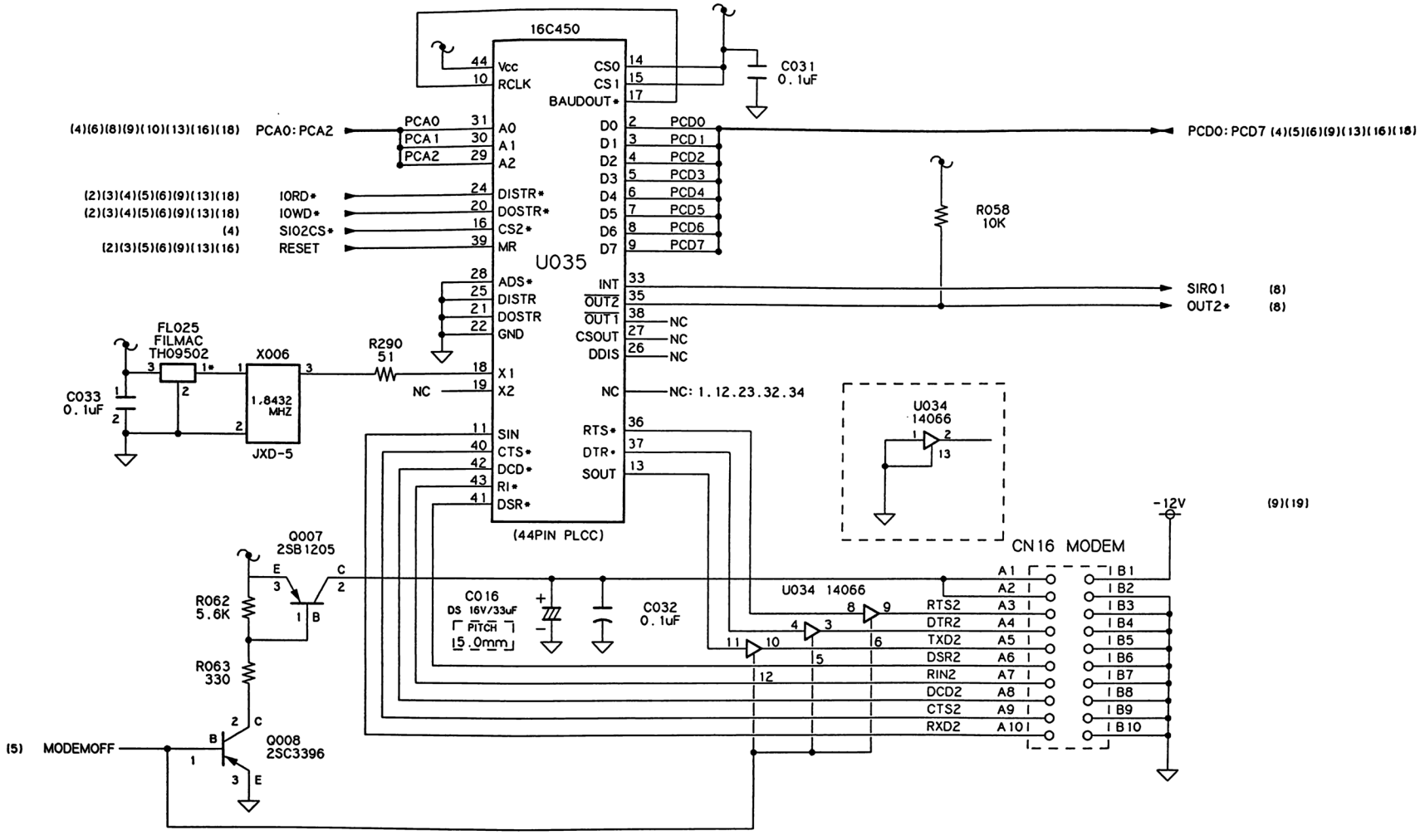
NOTE:	SIZE	MEMORY	UNIT	BANK
	1 MB	256Kx4	8	0, 1
	2 MB	1Mx4	4	0
*	4 MB	1Mx4	8	0, 1

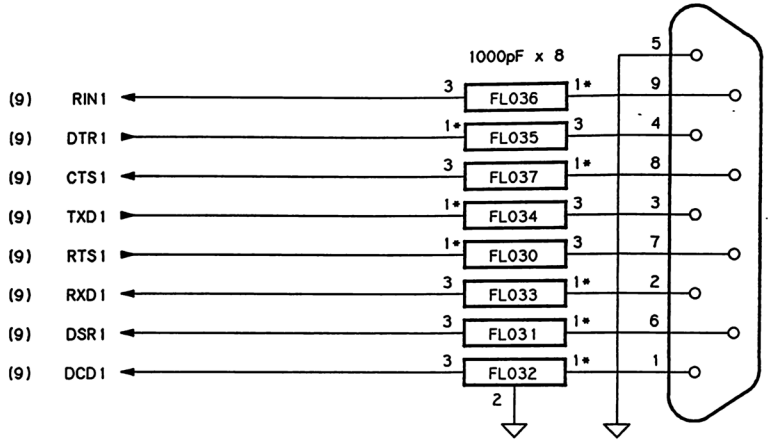


NOTE: J001~J003
<A> MEMORY 2M, 4M
<B> MEMORY 1M, 3M, 5M

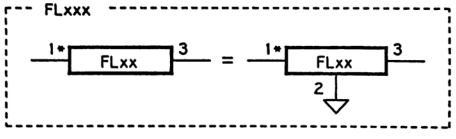
NOTE:	SIZE	MEMORY	UNIT	BANK
	3KB	1Mx4	4	2
	4KB	1Mx4	4	2
	5KB	1Mx4	8	2.3
*	8KB	1Mx4	8	2.3

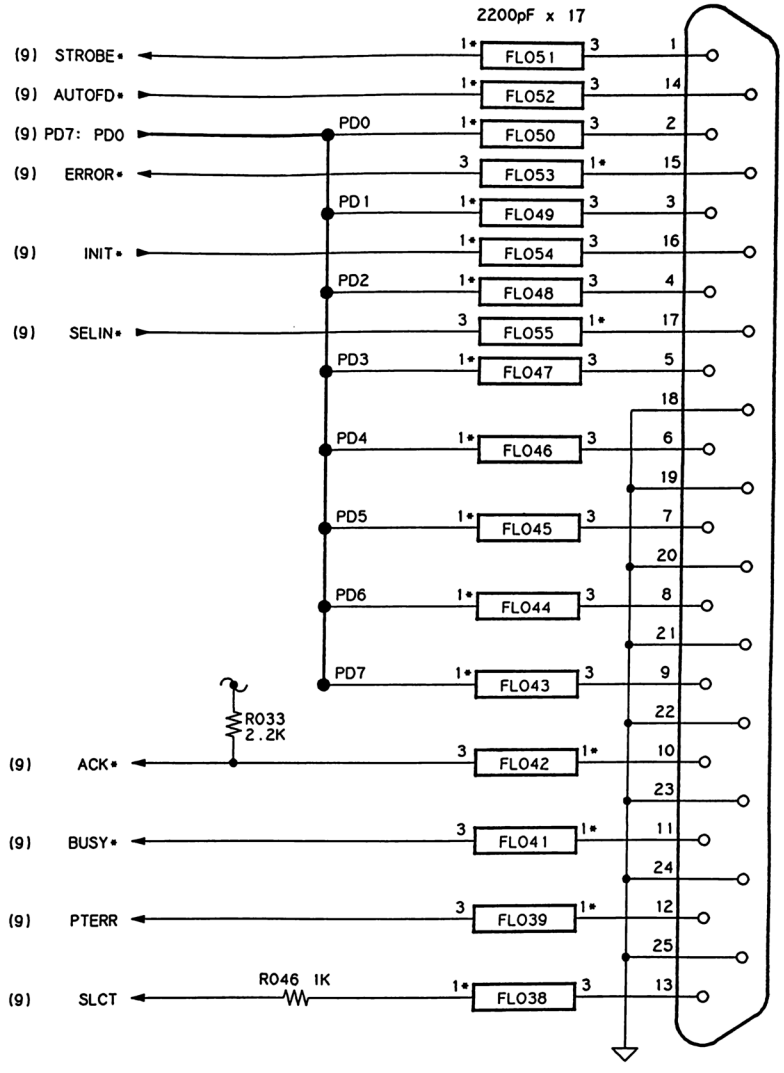

U022
WD37C65
(44IN PLCC)
C036
0.1uF
R088 10K
R084 2.2K
R086 10K
R085 10K
R087 10K
R089 10K
R289 51
C047
0.1µF
FILMAC
TH09502
FL016
X003
9.6MHz
JXO-5
PCD7 14
PCD6 13
PCD5 12
PCD4 11
PCD3 10
PCD2 9
PCD1 8
PCD0 7
D7
D6
D5
D4
D3
D2
D1
D0
(4)(5)(6)(9)(14)(16)(18) PCD7:PCD0
(8) LDCR* 19 LDCR
(8) LDOR* 18 LDOR
(4)(8)(9)(14)(16)(18) PCA0 4 A0
(8) FDCCS* 3 CS
(2)(3)(4)(5)(9)(14)(18) IORD* 1 RD
(2)(3)(4)(5)(9)(14)(18) IOWR* 2 WR
(3)(16) DRQ2 15 DRG
(3)(16) TC 6 TC
(9)(16) IRQ6 16 INT
(2)(3)(5)(6)(9)(14)(16) RESET 20 RESET
(3)(9)(16) DACK2* 5 DACK
(9) CRVTYPE 24 DRVTYP
27 PCVAL
23 XT2
26 XT1
NC 22 XT2*
NC 25 XT1*
17 DCHEN*
34 GND
(8) CLK16M
Vcc 44
WRTPRT 41
INDEX 43
TRK0 42
STEP 32
HDSEL 28
DIR 31
WDATA 30
WSATE 29
DSKCHG* 40
RDATA 21
DR0 33
DR1 35 NC
MTR0 36
MTR1 37 NC
HDL* 38 NC
RWC* 39 NC
WRTPRT* (18)
INDEX* (18)
TRK0* (18)
STEP* (18)
HEAD (18)
FLPDIR (18)
WDATA (18)
WGATE* (18)
DSKCHG* (18)
RDATA (18)
DRSELA* (18)(19)
MTENA* (18)


16C450
U035
(44PIN PLCC)
Vcc
RCLK
CS0
CS1
BAUDOUT*
PCA0
PCA1
PCA2
A0
A1
A2
D0
D1
D2
D3
D4
D5
D6
D7
PCD0
PCD1
PCD2
PCD3
PCD4
PCD5
PCD6
PCD7
PCA0: PCA2
PCD0: PCD7
IORD*
IOWD*
SIO2CS*
RESET
DISTR*
DOSTR*
CS2*
MR
ADS*
DISTR
DOSTR
GND
INT
OUT2
OUT1
CSOUT
DDIS
X1
X2
NC
NC: 1.12.23.32.34
SIN
CTS*
DCD*
RI*
DSR*
RTS*
DTR*
SOUT
SIRQ1
OUT2*
C031
0.1uF
R058
10K
R290
51
FL025
FILMAC
TH09502
X006
1.8432
MHZ
JXD-5
C033
0.1uF
U034
14066
-12V
Q007
2SB1205
R062
5.6K
R063
330
Q008
2SC3396
MODEMOFF
C016
DS 16V/33uF
PITCH
15.0mm
C032
0.1uF
U034 14066
CN16 MODEM
RTS2
DTR2
TXD2
DSR2
RIN2
DCD2
CTS2
RXD2

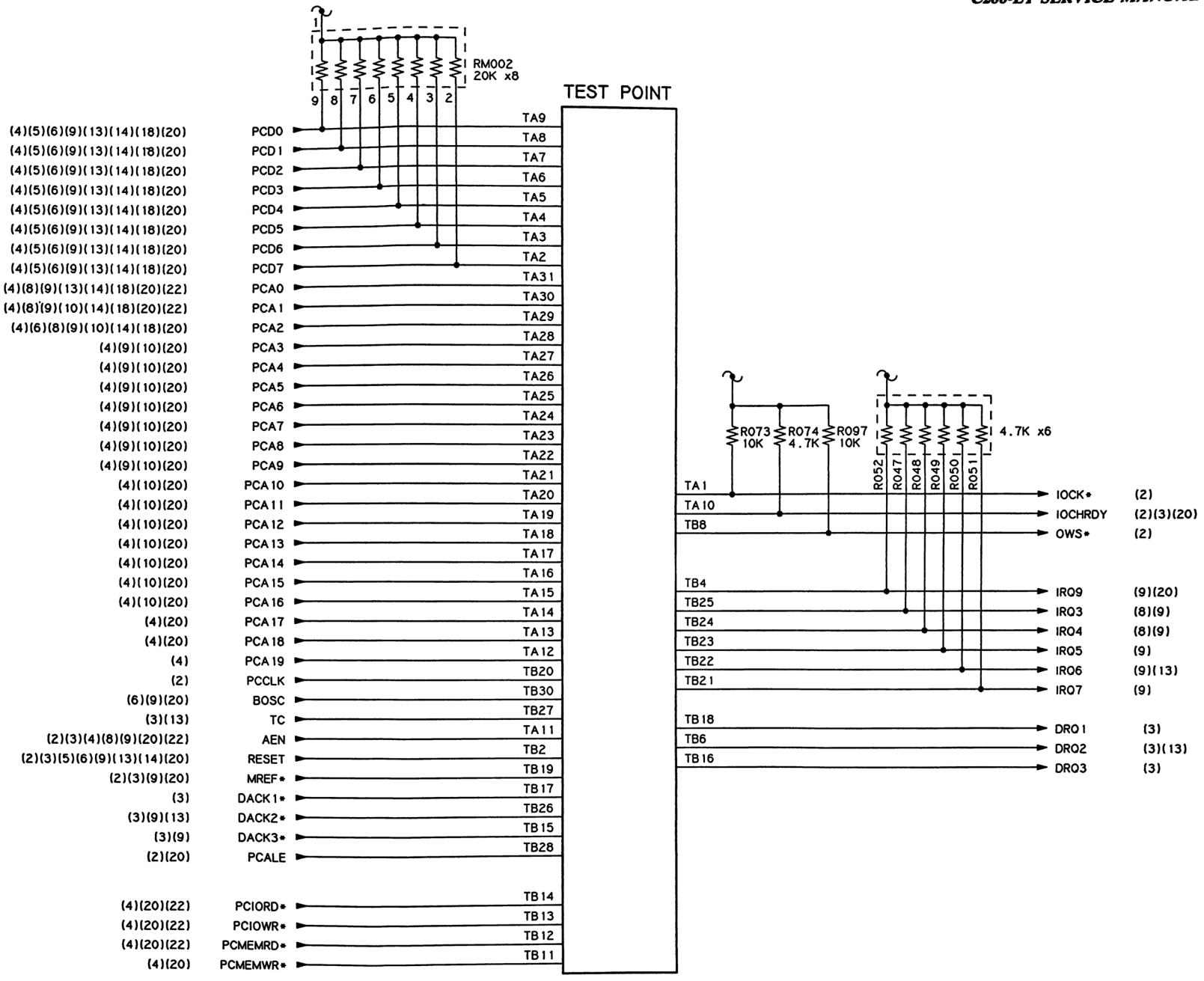


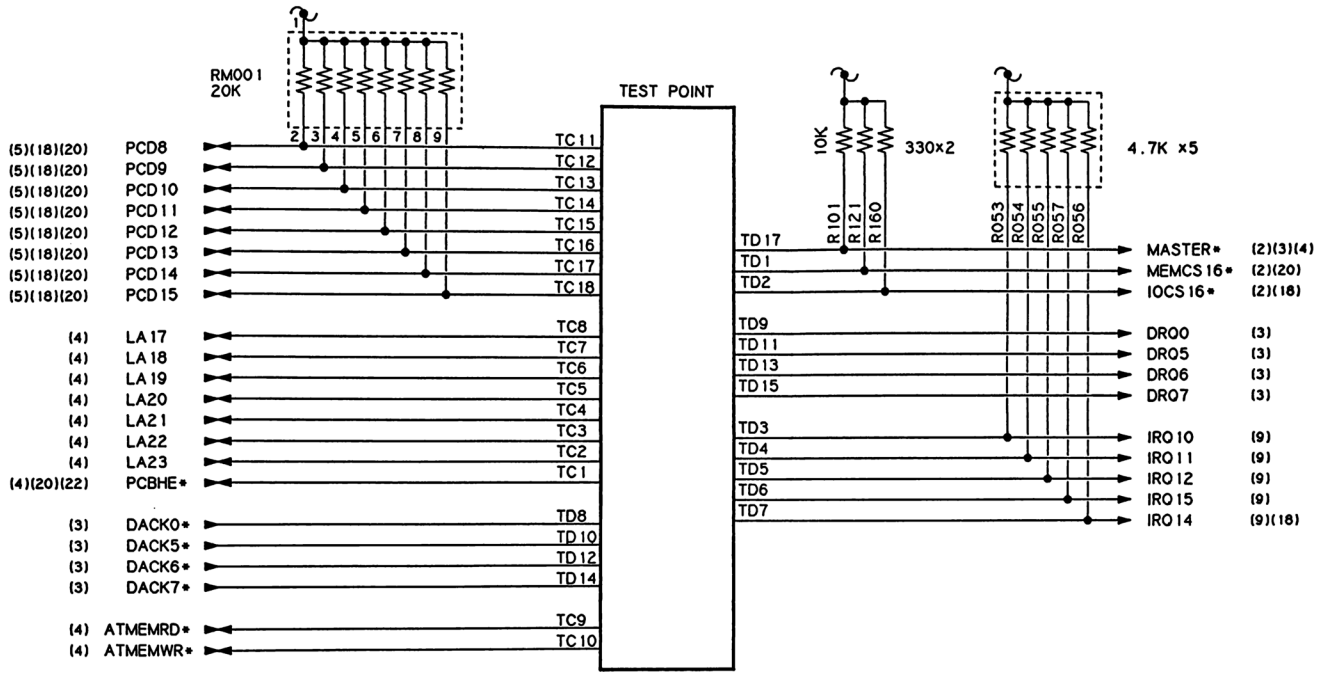
CN14 RS-232C

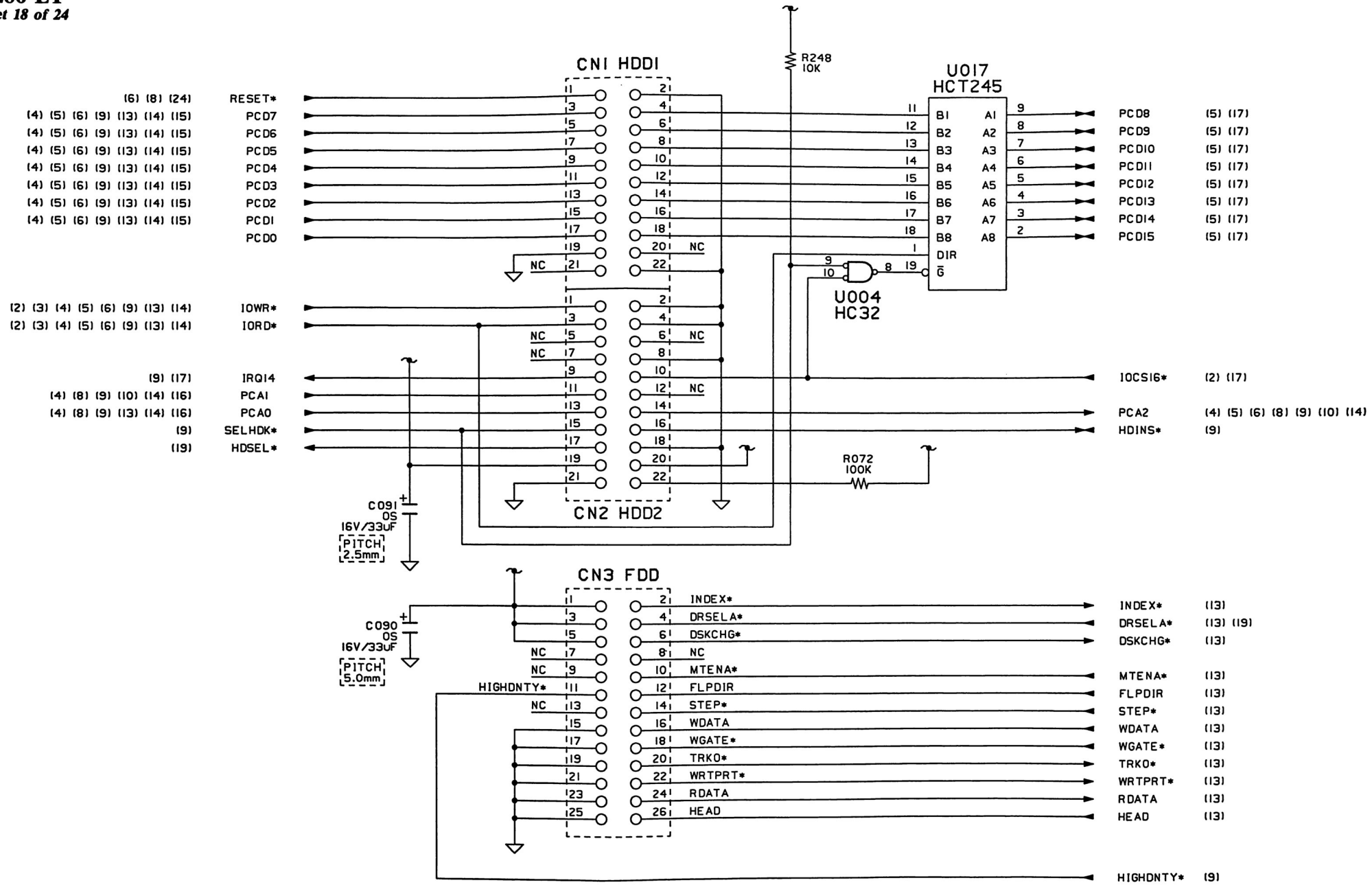


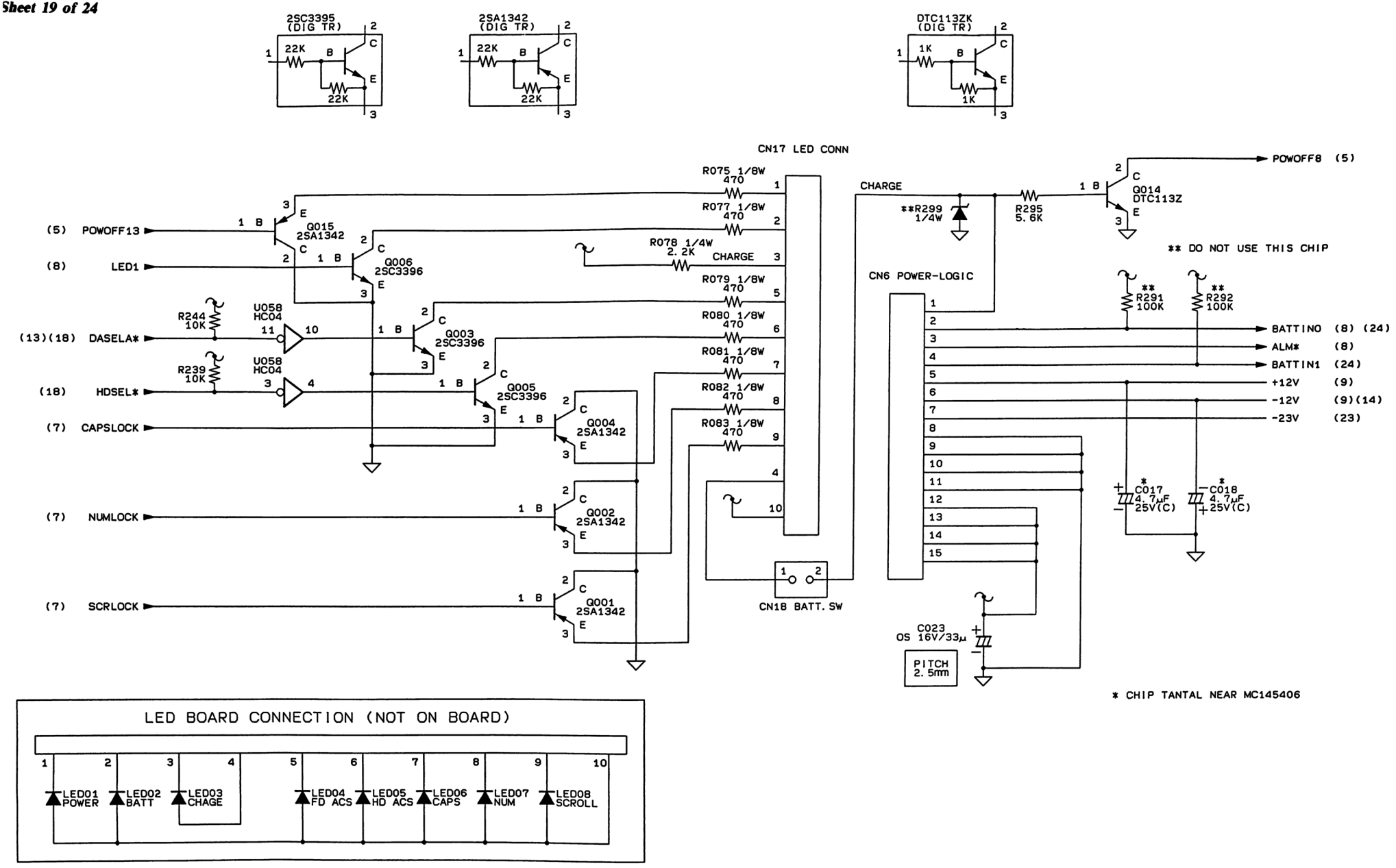


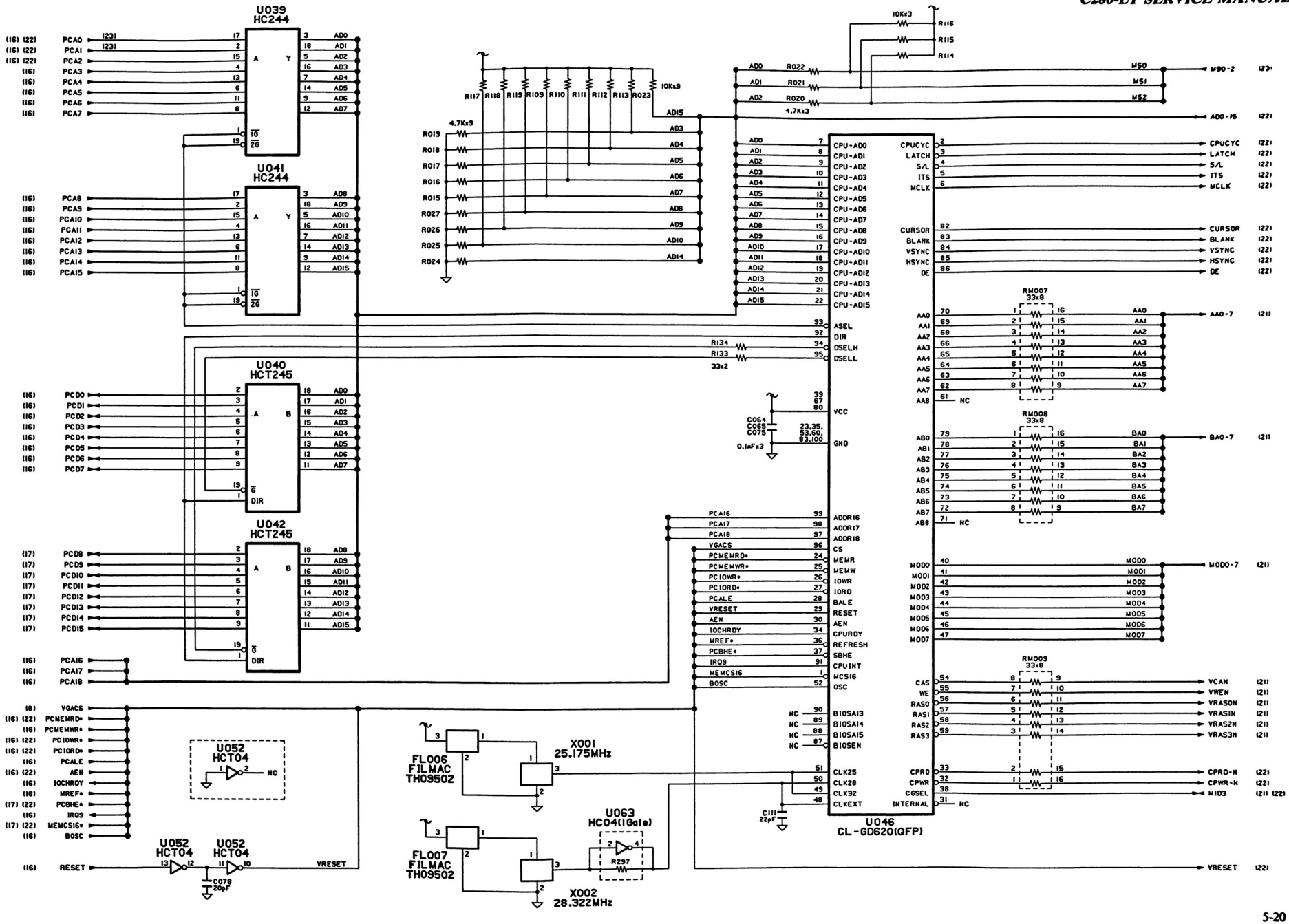
CN15 PARALLEL

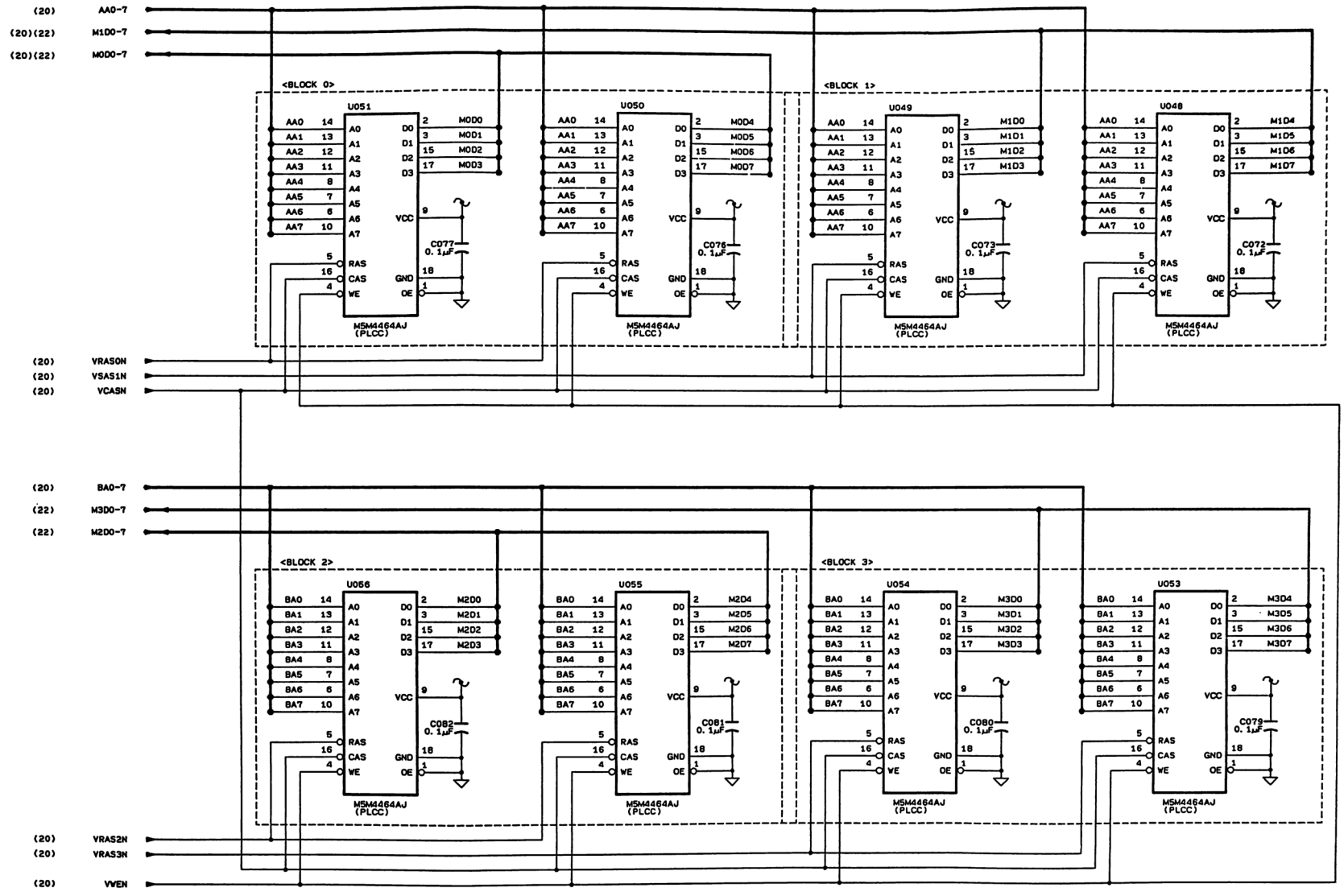

RM002
20K x8
1
9 8 7 6 5 4 3 2
TEST POINT
(4)(5)(6)(9)(13)(14)(18)(20) PCD0 TA9
(4)(5)(6)(9)(13)(14)(18)(20) PCD1 TA8
(4)(5)(6)(9)(13)(14)(18)(20) PCD2 TA7
(4)(5)(6)(9)(13)(14)(18)(20) PCD3 TA6
(4)(5)(6)(9)(13)(14)(18)(20) PCD4 TA5
(4)(5)(6)(9)(13)(14)(18)(20) PCD5 TA4
(4)(5)(6)(9)(13)(14)(18)(20) PCD6 TA3
(4)(5)(6)(9)(13)(14)(18)(20) PCD7 TA2
(4)(8)(9)(13)(14)(18)(20)(22) PCA0 TA31
(4)(8)(9)(10)(14)(18)(20)(22) PCA1 TA30
(4)(6)(8)(9)(10)(14)(18)(20) PCA2 TA29
(4)(9)(10)(20) PCA3 TA28
(4)(9)(10)(20) PCA4 TA27
(4)(9)(10)(20) PCA5 TA26
(4)(9)(10)(20) PCA6 TA25
(4)(9)(10)(20) PCA7 TA24
(4)(9)(10)(20) PCA8 TA23
(4)(9)(10)(20) PCA9 TA22
(4)(10)(20) PCA10 TA21
(4)(10)(20) PCA11 TA20
(4)(10)(20) PCA12 TA19
(4)(10)(20) PCA13 TA18
(4)(10)(20) PCA14 TA17
(4)(10)(20) PCA15 TA16
(4)(10)(20) PCA16 TA15
(4)(20) PCA17 TA14
(4)(20) PCA18 TA13
(4) PCA19 TA12
(2) PCCLK TB20
(6)(9)(20) BOSC TB30
(3)(13) TC TB27
(2)(3)(4)(8)(9)(20)(22) AEN TA11
(2)(3)(5)(6)(9)(13)(14)(20) RESET TB2
(2)(3)(9)(20) MREF* TB19
(3) DACK1* TB17
(3)(9)(13) DACK2* TB26
(3)(9) DACK3* TB15
(2)(20) PCALE TB28
(4)(20)(22) PCIORD* TB14
(4)(20)(22) PCIOWR* TB13
(4)(20)(22) PCMEMRD* TB12
(4)(20) PCMEMWR* TB11
R073 10K
R074 4.7K
R097 10K
4.7K x6
R052 R047 R048 R049 R050 R051
TA1 IOCK* (2)
TA10 IOCHRDY (2)(3)(20)
TB8 OWS* (2)
TB4 IRQ9 (9)(20)
TB25 IRQ3 (8)(9)
TB24 IRQ4 (8)(9)
TB23 IRQ5 (9)
TB22 IRQ6 (9)(13)
TB21 IRQ7 (9)
TB18 DRQ1 (3)
TB6 DRQ2 (3)(13)
TB16 DRQ3 (3)

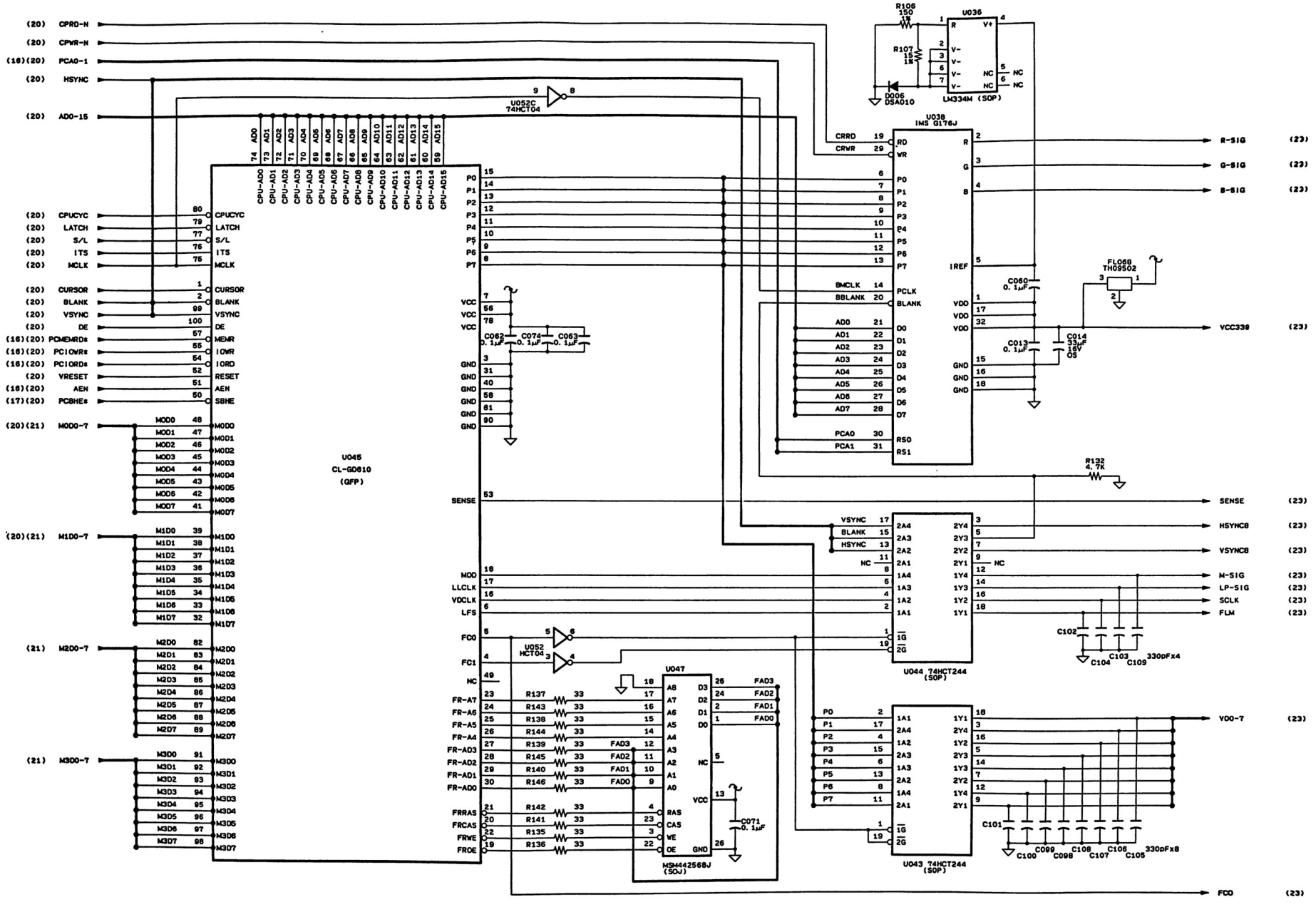

RM001
20K
1
2 3 4 5 6 7 8 9
TEST POINT
10K
330x2
4.7K x5
R101
R121
R160
R053
R054
R055
R057
R056
(5)(18)(20) PCD8
(5)(18)(20) PCD9
(5)(18)(20) PCD10
(5)(18)(20) PCD11
(5)(18)(20) PCD12
(5)(18)(20) PCD13
(5)(18)(20) PCD14
(5)(18)(20) PCD15
(4) LA17
(4) LA18
(4) LA19
(4) LA20
(4) LA21
(4) LA22
(4) LA23
(4)(20)(22) PCBHE*
(3) DACK0*
(3) DACK5*
(3) DACK6*
(3) DACK7*
(4) ATMEMRD*
(4) ATMEMWR*
TC11
TC12
TC13
TC14
TC15
TC16
TC17
TC18
TC8
TC7
TC6
TC5
TC4
TC3
TC2
TC1
TD8
TD10
TD12
TD14
TC9
TC10
TD17
TD1
TD2
TD9
TD11
TD13
TD15
TD3
TD4
TD5
TD6
TD7
MASTER* (2)(3)(4)
MEMCS16* (2)(20)
IOCS16* (2)(18)
DRO0 (3)
DRO5 (3)
DRO6 (3)
DRO7 (3)
IRO10 (9)
IRO11 (9)
IRO12 (9)
IRO15 (9)
IRO14 (9)(18)

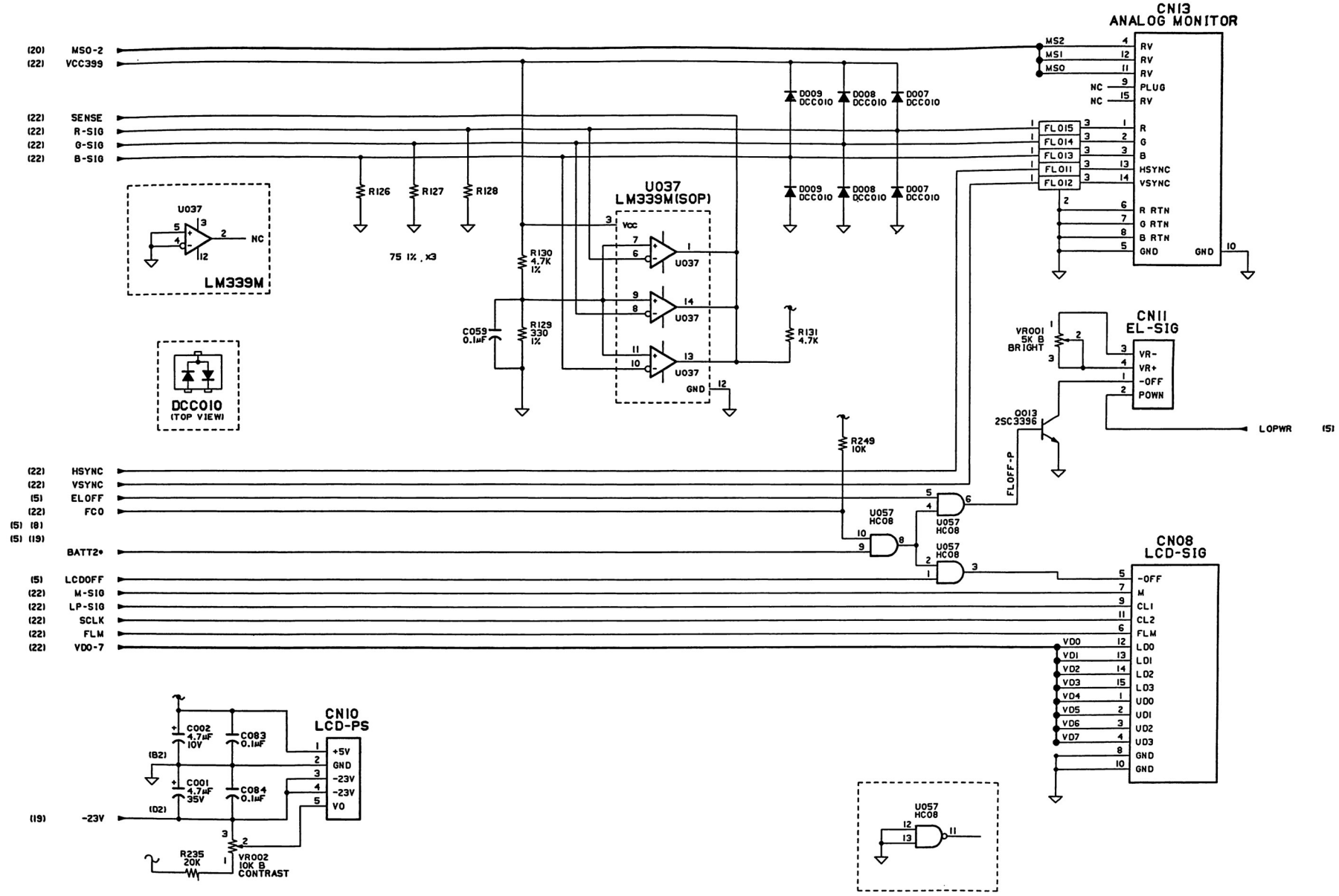

CN1 HDD1
R248
10K
U017
HCT245
U004
HC32
CN2 HDD2
R072
100K
C091
OS
16V/33UF
PITCH
2.5mm
CN3 FDD
C090
OS
16V/33UF
PITCH
5.0mm
(6) (8) (24) RESET*
(4) (5) (6) (9) (13) (14) (15) PCD7
(4) (5) (6) (9) (13) (14) (15) PCD6
(4) (5) (6) (9) (13) (14) (15) PCD5
(4) (5) (6) (9) (13) (14) (15) PCD4
(4) (5) (6) (9) (13) (14) (15) PCD3
(4) (5) (6) (9) (13) (14) (15) PCD2
(4) (5) (6) (9) (13) (14) (15) PCD1
PCD0
(2) (3) (4) (5) (6) (9) (13) (14) IOWR*
(2) (3) (4) (5) (6) (9) (13) (14) IORD*
(9) (17) IRQ14
(4) (8) (9) (10) (14) (16) PCA1
(4) (8) (9) (13) (14) (16) PCA0
(9) SELHDK*
(19) HDSEL*
PCD8 (5) (17)
PCD9 (5) (17)
PCD10 (5) (17)
PCD11 (5) (17)
PCD12 (5) (17)
PCD13 (5) (17)
PCD14 (5) (17)
PCD15 (5) (17)
IOCS16* (2) (17)
PCA2 (4) (5) (6) (8) (9) (10) (14)
HDINS* (9)
INDEX*
DRSELA*
DSKCHG*
MTENA*
HIGHDNTY*
FLPDIR
STEP*
WDATA
WGATE*
TRK0*
WRTPRT*
RDATA
HEAD
INDEX* (13)
DRSELA* (13) (19)
DSKCHG* (13)
MTENA* (13)
FLPDIR (13)
STEP* (13)
WDATA (13)
WGATE* (13)
TRK0* (13)
WRTPRT* (13)
RDATA (13)
HEAD (13)
HIGHDNTY* (9)

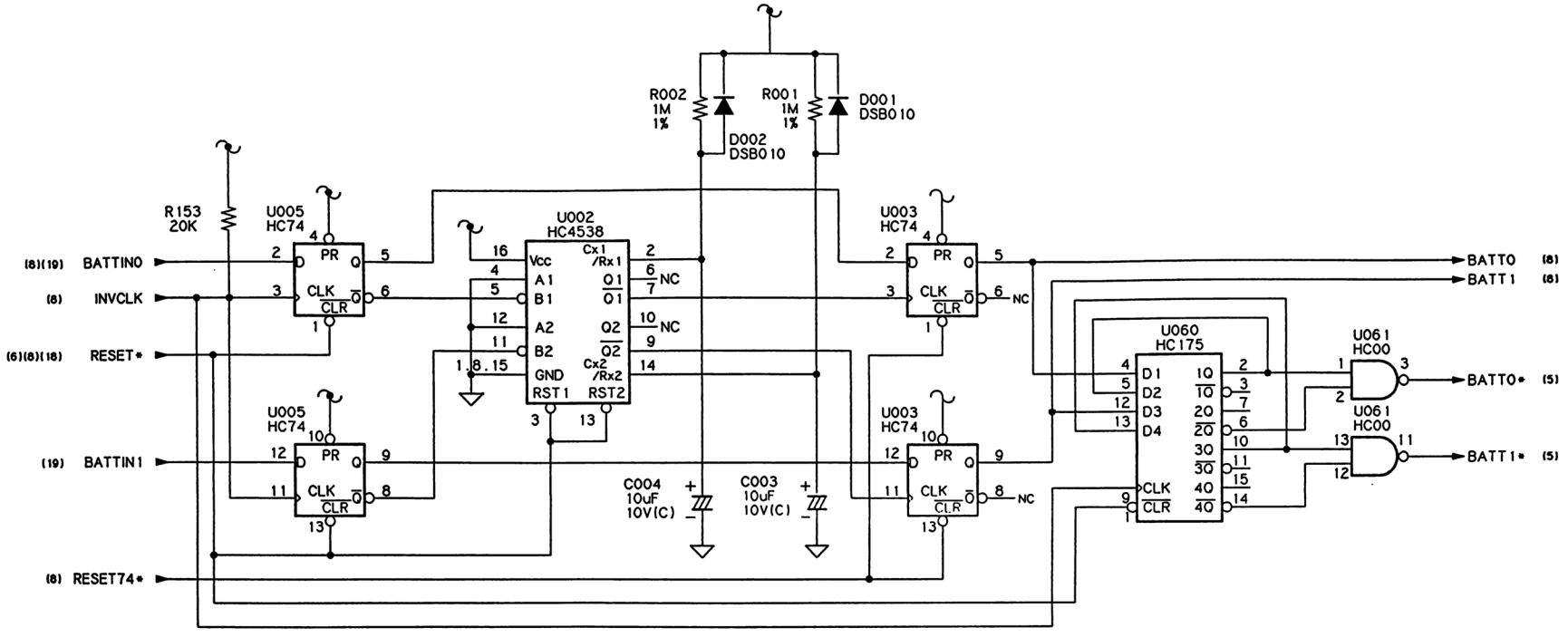

2SC3395 (DIG TR)
22K
22K
2SA1342 (DIG TR)
22K
22K
DTC113ZK (DIG TR)
1K
1K
CN17 LED CONN
(5) POWOFF13
(8) LED1
(13)(18) DASELA*
(18) HDSEL*
(7) CAPSLOCK
(7) NUMLOCK
(7) SCRLOCK
Q015 2SA1342
Q006 2SC3396
Q003 2SC3396
Q005 2SC3396
Q004 2SA1342
Q002 2SA1342
Q001 2SA1342
U058 HC04
U058 HC04
R244 10K
R239 10K
R075 1/8W 470
R077 1/8W 470
R078 1/4W 2.2K
R079 1/8W 470
R080 1/8W 470
R081 1/8W 470
R082 1/8W 470
R083 1/8W 470
CHARGE
CN18 BATT. SW
CHARGE
**R299 1/4W
R295 5.6K
Q014 DTC113Z
POWOFF8 (5)
** DO NOT USE THIS CHIP
CN6 POWER-LOGIC
** R291 100K
** R292 100K
BATTINO (8) (24)
ALM* (8)
BATTIN1 (24)
+12V (9)
-12V (9)(14)
-23V (23)
* C017 4.7μF 25V(C)
* C018 4.7μF 25V(C)
C023 OS 16V/33μ
PITCH 2.5mm
* CHIP TANTAL NEAR MC145406
LED BOARD CONNECTION (NOT ON BOARD)
LED01 POWER
LED02 BATT
LED03 CHAGE
LED04 FD ACS
LED05 HD ACS
LED06 CAPS
LED07 NUM
LED08 SCROLL


U039
HC244
U041
HC244
U040
HCT245
U042
HCT245
U046
CL-GD620(QFP)
U052
HCT04
U063
HC04(1Gate)
X001
25.175MHz
X002
28.322MHz
FL006
FILMAC
TH09502
FL007
FILMAC
TH09502
RM007
33x8
RM008
33x8
RM009
33x8
10Kx3
4.7Kx3
4.7Kx9
10Kx9
33x2
0.1mFx3
C078
20pF
C111
22pF
R297
PCA0
PCA1
PCA2
PCA3
PCA4
PCA5
PCA6
PCA7
PCA8
PCA9
PCA10
PCA11
PCA12
PCA13
PCA14
PCA15
PCA16
PCA17
PCA18
PCD0
PCD1
PCD2
PCD3
PCD4
PCD5
PCD6
PCD7
PCD8
PCD9
PCD10
PCD11
PCD12
PCD13
PCD14
PCD15
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
VGACS
PCMEMRD*
PCMEMWR*
PCIOWR*
PCIORD*
PCALE
AEN
IOCHRDY
MREF*
PCBHE*
IRQ9
MEMCS16*
BOSC
RESET
VRESET
CPU-AD0
CPU-AD1
CPU-AD2
CPU-AD3
CPU-AD4
CPU-AD5
CPU-AD6
CPU-AD7
CPU-AD8
CPU-AD9
CPU-AD10
CPU-AD11
CPU-AD12
CPU-AD13
CPU-AD14
CPU-AD15
ASEL
DIR
DSELH
DSELL
VCC
GND
ADDR16
ADDR17
ADDR18
CS
MEMR
MEMW
IOWR
IORD
BALE
RESET
AEN
CPURDY
REFRESH
SBHE
CPUINT
MCS16
OSC
BIOSAI3
BIOSAI4
BIOSAI5
BIOSEN
CLK25
CLK28
CLK32
CLKEXT
CPUCYC
LATCH
S/L
ITS
MCLK
CURSOR
BLANK
VSYNC
HSYNC
DE
AA0-7
BA0-7
MD0-7
VCAN
VWEN
VRASON
VRASIN
VRAS2N
VRAS3N
CPRD-N
CPWR-N
MIO3
INTERNAL
MS0-2
AD0-15


(20) AA0-7
(20)(22) M1D0-7
(20)(22) M0D0-7
<BLOCK 0>
<BLOCK 1>
U051
U050
U049
U048
M5M4464AJ (PLCC)
C077 0.1μF
C078 0.1μF
C073 0.1μF
C072 0.1μF
(20) VRASON
(20) VSAS1N
(20) VCASN
(20) BA0-7
(22) M3D0-7
(22) M2D0-7
<BLOCK 2>
<BLOCK 3>
U056
U055
U054
U053
C082 0.1μF
C081 0.1μF
C080 0.1μF
C079 0.1μF
(20) VRAS2N
(20) VRAS3N
(20) VWEN


(20) CPRD-N
(20) CPWR-N
(16)(20) PCA0-1
(20) HSYNC
(20) AD0-15
(20) CPUCYC
(20) LATCH
(20) S/L
(20) ITS
(20) MCLK
(20) CURSOR
(20) BLANK
(20) VSYNC
(20) DE
(16)(20) PCMEMRD#
(16)(20) PCIOWR#
(16)(20) PCIORD#
(20) VRESET
(16)(20) AEN
(17)(20) PCBHE#
(20)(21) MOD0-7
(20)(21) M1D0-7
(21) M2D0-7
(21) M3D0-7
U045
CL-GD610
(QFP)
U052C
74HCT04
U052
HCT04
U047
MSM442568J
(SOJ)
U038
IMS G176J
U044 74HCT244
(SOP)
U043 74HCT244
(SOP)
U036
LM334M (SOP)
D006
DSA010
R106
150
R107
15
R132
4.7K
FL068
TH09502
C060
0.1µF
C013
0.1µF
C014
33µF
16V
OS
C062
0.1µF
C074
0.1µF
C063
0.1µF
C102
C103
C104
C109
330pFx4
C101
C100
C099
C098
C108
C107
C106
C105
330pFx8
C071
0.1µF
R-SIG (23)
G-SIG (23)
B-SIG (23)
VCC330 (23)
SENSE (23)
HSYNC8 (23)
VSYNC8 (23)
M-SIG (23)
LP-SIG (23)
SCLK (23)
FLM (23)
VD0-7 (23)
FC0 (23)


CN13
ANALOG MONITOR
(20) MSO-2
(22) VCC399
(22) SENSE
(22) R-SIG
(22) G-SIG
(22) B-SIG
MS2
MS1
MSO
NC
NC
RV
RV
RV
PLUG
RV
R
G
B
HSYNC
VSYNC
R RTN
G RTN
B RTN
GND
GND
FL015
FL014
FL013
FL011
FL012
D009 DCC010
D008 DCC010
D007 DCC010
R126
R127
R128
75 1%, x3
U037
LM339M(SOP)
VCC
GND
R130 4.7K 1%
R129 330 1%
C059 0.1uF
R131 4.7K
U037
LM339M
NC
DCC010
(TOP VIEW)
CN11
EL-SIG
VR001 5K B BRIGHT
VR-
VR+
-OFF
POWN
Q013 2SC3396
LOPWR (5)
R249 10K
FLOFF-P
(22) HSYNC
(22) VSYNC
(5) ELOFF
(22) FCO
(5) (8)
(5) (19)
BATT2+
U057 HC08
(5) LCDOFF
(22) M-SIG
(22) LP-SIG
(22) SCLK
(22) FLM
(22) VD0-7
CN08
LCD-SIG
-OFF
M
CL1
CL2
FLM
LD0
LD1
LD2
LD3
UD0
UD1
UD2
UD3
GND
GND
VD0
VD1
VD2
VD3
VD4
VD5
VD6
VD7
CN10
LCD-PS
+5V
GND
-23V
-23V
VO
C002 4.7uF 10V
C083 0.1uF
C001 4.7uF 35V
C084 0.1uF
(B2)
(D2)
(19) -23V
R235 20K
VR002 10K B CONTRAST


R002
1M
1%
R001
1M
1%
D001
DSB010
D002
DSB010
R153
20K
U005
HC74
U002
HC4538
U003
HC74
U060
HC175
U061
HC00
U061
HC00
(8)(19) BATTIN0
(8) INVCLK
(6)(8)(18) RESET*
(19) BATTIN1
(8) RESET74*
C004
10uF
10V(C)
C003
10uF
10V(C)
BATT0 (8)
BATT1 (8)
BATT0* (5)
BATT1* (5)

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